

ZR6 SYSTEM BLOCK DIAGRAM

BOM MARK
IV@: INT VGA
EV@: STUFF FOR EXT VGA
SP@: STUFF FOR UMA or VGA

REV:C

DDR3 PWR TPS51116 P36	CHARGER ISL6251 P32
THERMAL PROTECTION P40	3/5V SYS PWR ISL6237 P33
DISCHARGER P39	CPU CORE PWR OZ8116LN P35
VGA CORE OZ8118 P37	+1.05V UP6111AQDD P34

CLOCK GENERATOR
ICS:
SELGO: SLG8SP512TTR P2

XTAL
14.318MHz

Penryn 479
uFCPGA P3, P4

Thermal Sensor
(G780-1P81U) P3

Fan Driver
(G991) P25

DDRIII
SO-DIMM 0
SO-DIMM 1 P16

NB Cantiga
(GM45/ PM45/ GL40)
P5, P6, P7, P8, P9, P10, P11

NVIDIA N10M-GE1
VRAM DDRII 512MB P17-P23

SWITCH CIRCUIT
P24

HDMI switch (PS8101T)
P24

CRT
P24

LVDS
P24

HDMI
P24

HDD (SATA) *1
P25

ODD (SATA)
P25

SB ICH9M
P12,P13,P14,P15

PCI-Express

PCI-E-1

Mini Card WLAN
P26

Ext USB Port x 2
USB 0,1 P26

Int USB Port x 1
USB 7 P26

Bluetooth
USB5 P26

CCD
USB11 P24

Audio CODEC (CX20561)
P27

Audio Amplifier G1453L
P27

MIC Jack
P27

Int. MIC
P27

Int. Speaker
P27

EC (WPC775LDG)
P31

SPI ROM
P31

Touch Pad
P25

K/B COON.
P31

Media Cardreader (RTS5159)
USB2 P30

Card Reader Connector
P30

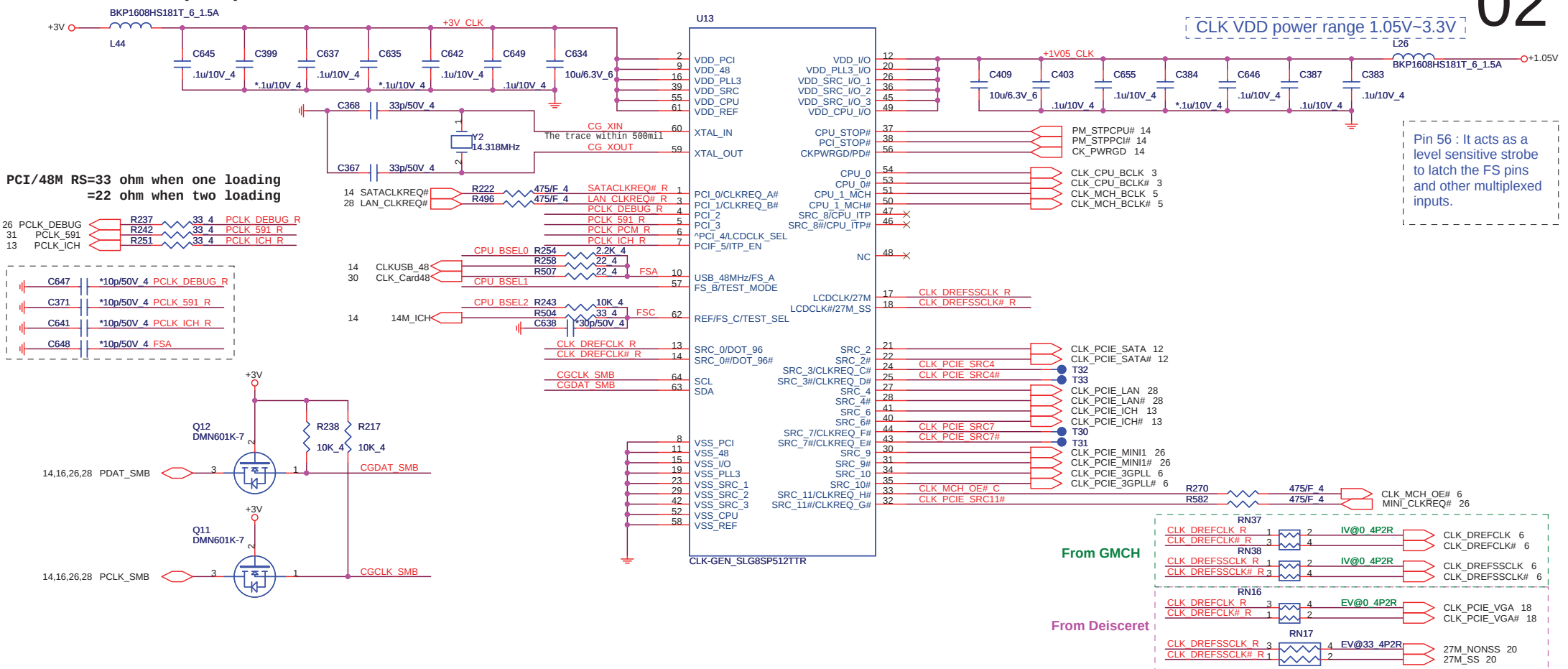
Atheros Giga-LAN (AR8131)
P28

Transformer
P29

RJ45
P29

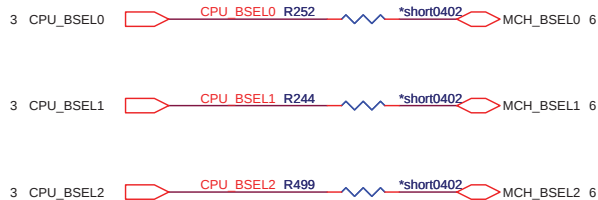
<http://hobi-elektronika.net>

Clock Generator (CLK)



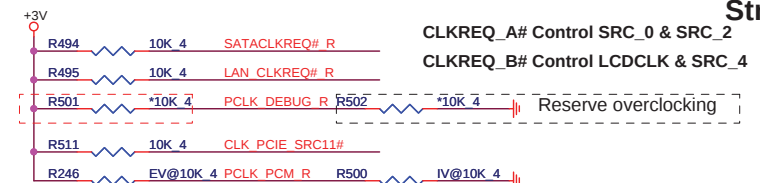
CPU Clock select

Pin 10/57/62 : For Pin CPU frequency selection



BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



Pin 6 : For Pin 13/14 and 17/18 selection
0 = LCDCLK & DOT96 for internal graphic controller support
1 = 27M & 27M_SS & SRC 0 for external graphic controller support

Pin 7 : For Pin 46/47 selection
1 = CPU_ITP
0 = SRC_8

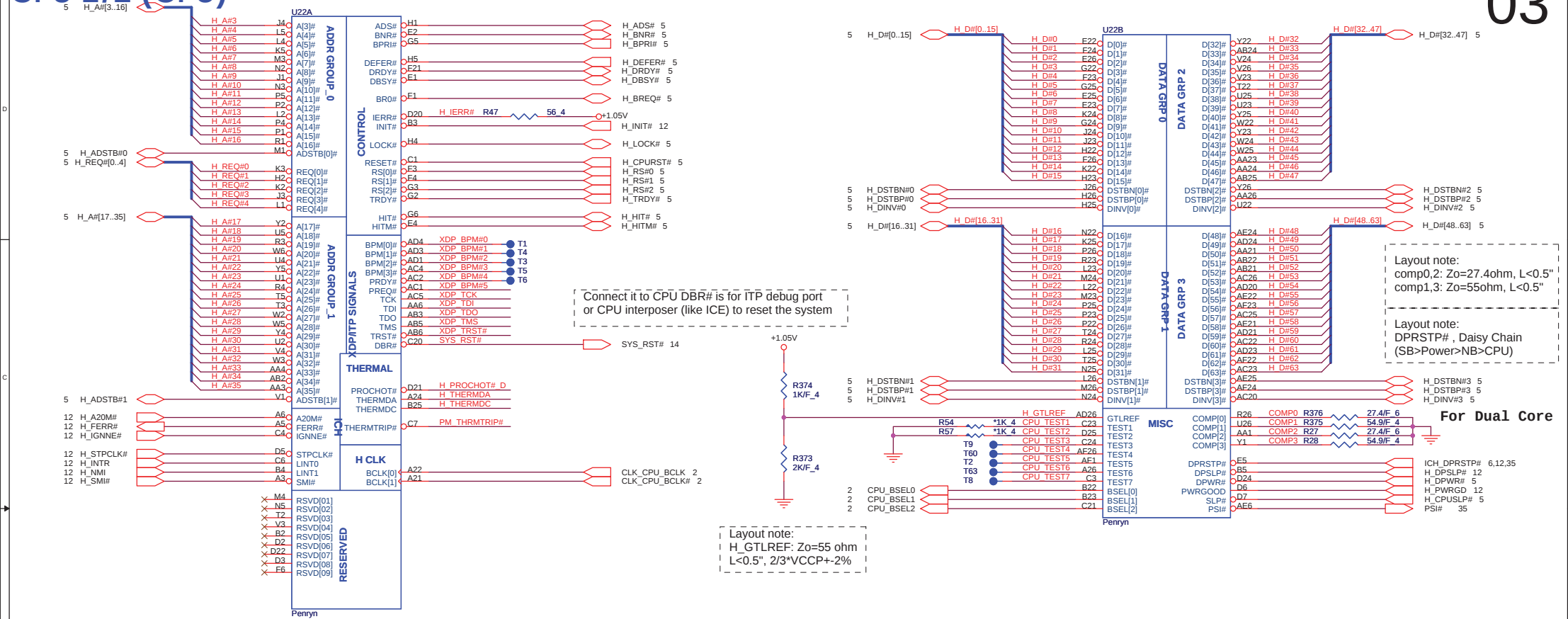
Strap table



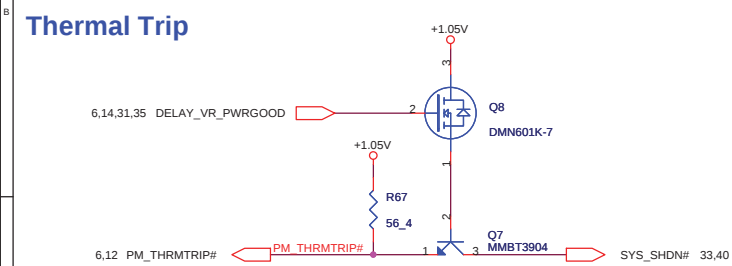
Quanta Computer Inc.
PROJECT : ZR6

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	CLOCK GENERATOR	1A
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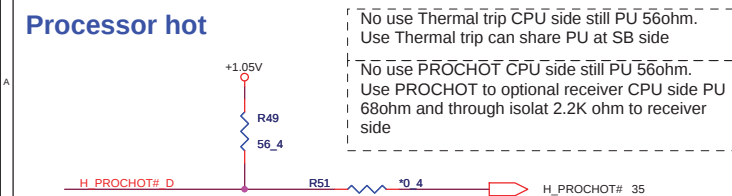
CPU 1/2 (CPU)



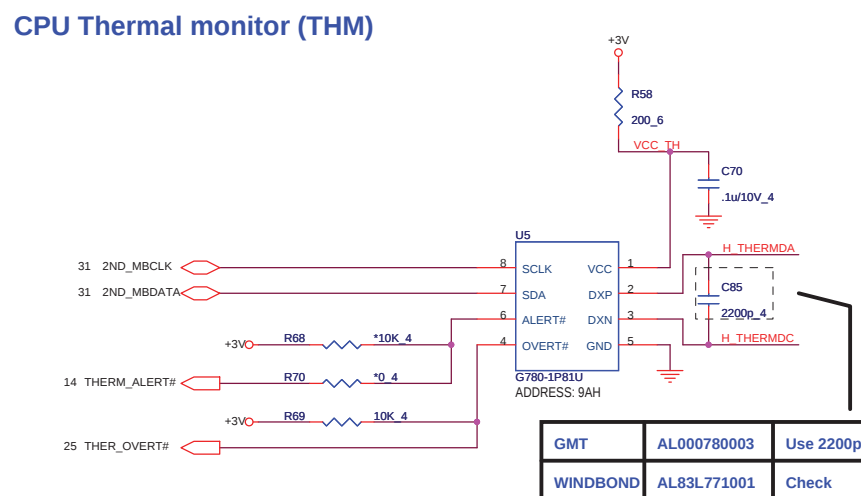
Thermal Trip



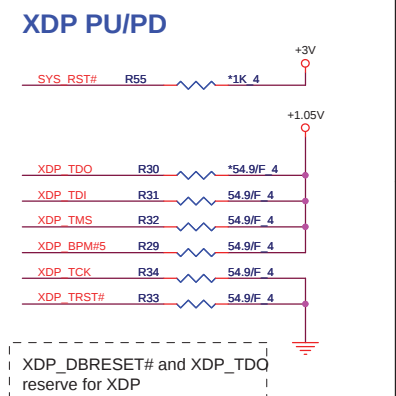
Processor hot



CPU Thermal monitor (THM)



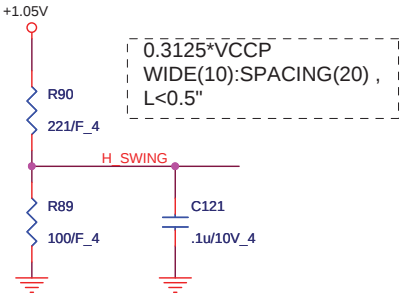
XDP PU/PD



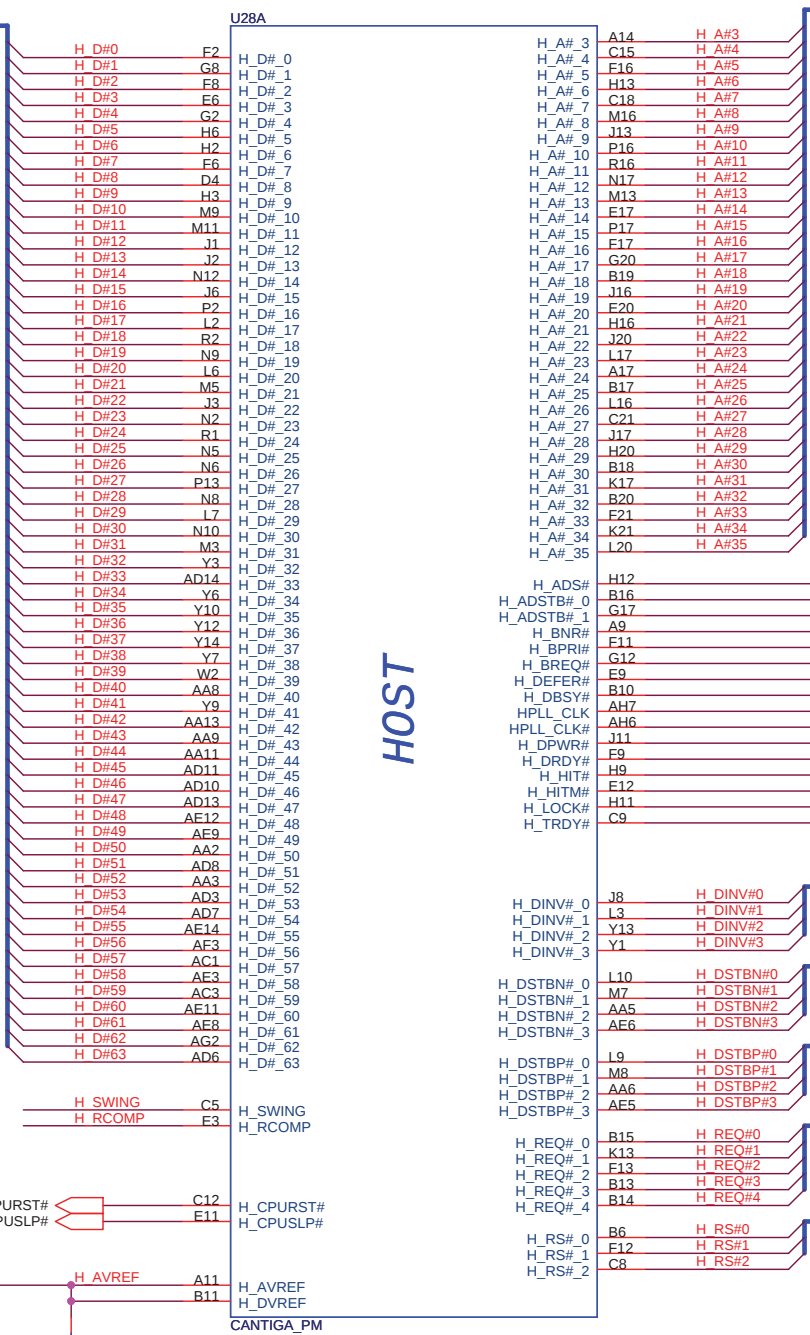
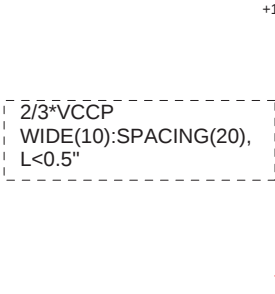
Quanta Computer Inc.
PROJECT : ZR6

GMCH-CANTIGA(CLG)

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06
Intel Cantiga (G)L A1	AJSLGGM0T04



Layout Note:
WIDE(10):SPACING(20),
L<0.5"



HOST



Quanta Computer Inc.

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GMCH HOST

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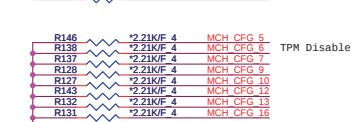
GMCH-CANTIGA(CLG)

IV@
EV@

Strap table

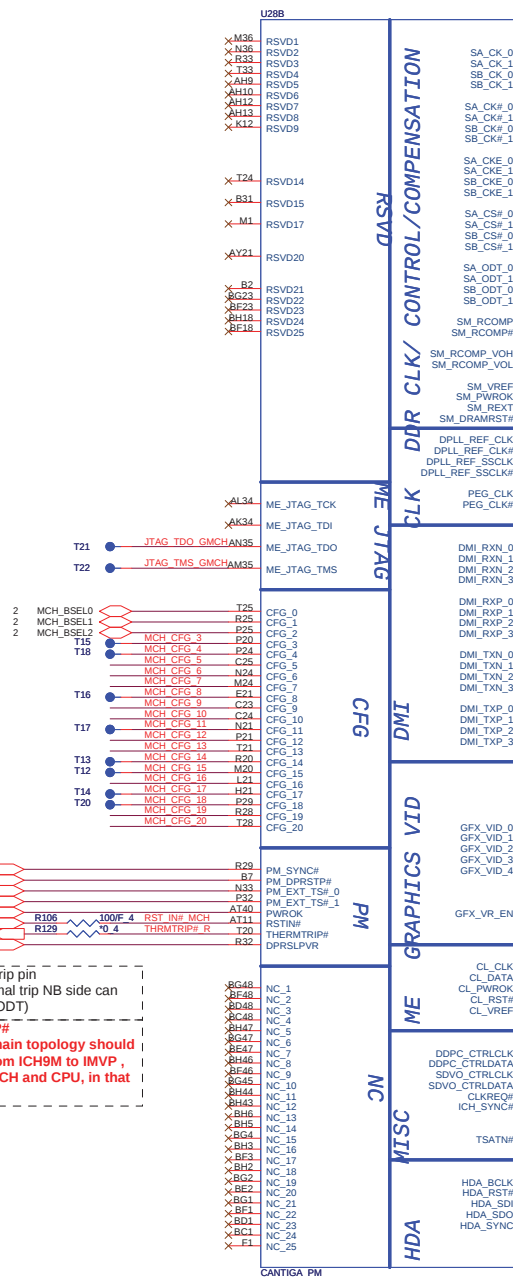
Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIe Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) and Concurrent with PCIe	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIe is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

Strap pin

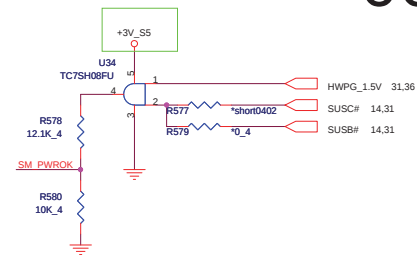


NB Thermal trip pin
No use Thermal trip NB side can NC.(NB has ODT)

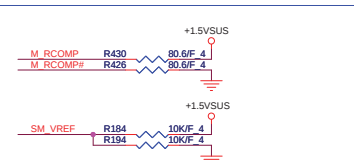
PM DPRSTP#
The Daisy chain topology should be routed from ICH9M to IMVP, then to (GMCH and CPU), in that order.



CANTIGA_PM

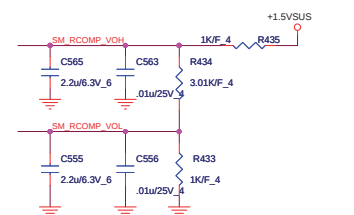
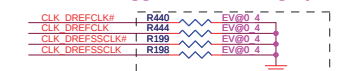


SM_VREF=0.5*VCC_SM
SM_PWROK only for DDR3.(DDR2 PD only)
SM_DRAMRST# only for DDR3.(DDR2-NC)

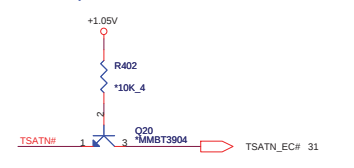


SM_VREF.Default use voltage divider for poor layout cause +SMDDR_VREF not meet spec.And Intel circuit PU/PD is 1K,But Check list PU/PD is 10K.

INTEL FAE Suggest PD for Ext graphics



NB Thermaltrip



DDPC_CTRL# for HDMI port C
SDVO_CTRL# for HDMI port B

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

<Pin out check issue>
Cantiga EDS 0.7 change Ball B12 to TSATN# from TSATN

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

<http://hobi-elektronika.net>

GMCH-CANTIGA(CLG)

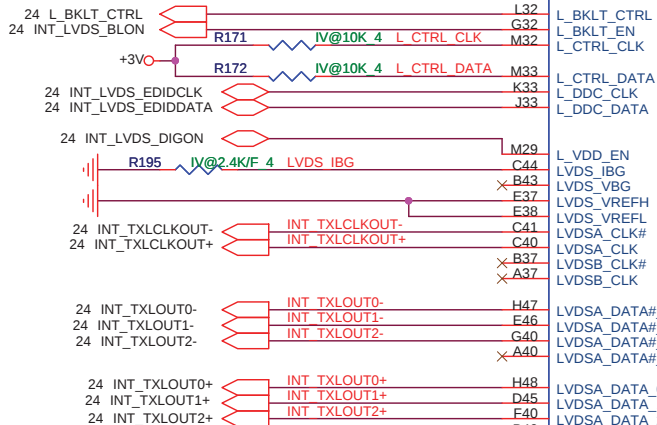
IV&EV Dis/Enable setting

If LVDS no use, all signal can NC

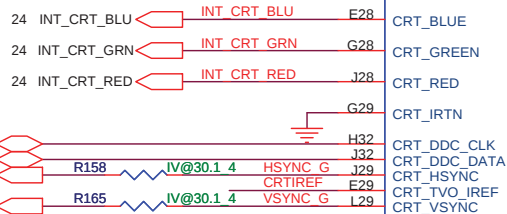
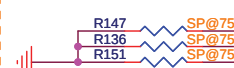
IV@

EV@

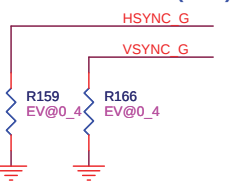
SP@



SP@
TV_A/B/C
For IV: 75ohm
For EV:0ohm



Discrete Stuffed. (CRT)



CRTIREF pull down
for IV cantiga 1.02k ohm/F

U28C

SDA7
PCI-EXPRESS
VGA

PEG_COMPI
PEG_COMPO

PEG_RX#_0
PEG_RX#_1
PEG_RX#_2
PEG_RX#_3
PEG_RX#_4
PEG_RX#_5
PEG_RX#_6
PEG_RX#_7
PEG_RX#_8
PEG_RX#_9
PEG_RX#_10
PEG_RX#_11
PEG_RX#_12
PEG_RX#_13
PEG_RX#_14
PEG_RX#_15

PEG_RX_0
PEG_RX_1
PEG_RX_2
PEG_RX_3
PEG_RX_4
PEG_RX_5
PEG_RX_6
PEG_RX_7
PEG_RX_8
PEG_RX_9
PEG_RX_10
PEG_RX_11
PEG_RX_12
PEG_RX_13
PEG_RX_14
PEG_RX_15

PEG_TX#_0
PEG_TX#_1
PEG_TX#_2
PEG_TX#_3
PEG_TX#_4
PEG_TX#_5
PEG_TX#_6
PEG_TX#_7
PEG_TX#_8
PEG_TX#_9
PEG_TX#_10
PEG_TX#_11
PEG_TX#_12
PEG_TX#_13
PEG_TX#_14
PEG_TX#_15

PEG_TX_0
PEG_TX_1
PEG_TX_2
PEG_TX_3
PEG_TX_4
PEG_TX_5
PEG_TX_6
PEG_TX_7
PEG_TX_8
PEG_TX_9
PEG_TX_10
PEG_TX_11
PEG_TX_12
PEG_TX_13
PEG_TX_14
PEG_TX_15

L<0.5", If PCIE not support
still connect to +VCC_PEG



Can support reversal routing. If CFG9=1, PCI Express
is normal operation. If CFG9=0, then PEG_TXP0
becomes PEG_TXP15, PEG_TXP1 becomes
PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc.
similarly for PEG_RXP[15:0] and PEG_RXN[15:0]

J41 C PEG TXN0 C583
M46 C PEG TXN1 C587
M47 C PEG TXN2 C591
M40 C PEG TXN3 C596
M42 C PEG TXN4 C618
R48 C PEG TXN5 C588
N38 C PEG TXN6 C600
T40 C PEG TXN7 C598
U37 C PEG TXN8 C604
U40 C PEG TXN9 C603
Y40 C PEG TXN10 C608
AA46 C PEG TXN11 C594
AA37 C PEG TXN12 C616
AA40 C PEG TXN13 C619
AD43 C PEG TXN14 C614
AC46 C PEG TXN15 C593

J42 C PEG TXP0 C580
L46 C PEG TXP1 C585
M48 C PEG TXP2 C590
M39 C PEG TXP3 C597
M43 C PEG TXP4 C611
R47 C PEG TXP5 C586
N37 C PEG TXP6 C601
T39 C PEG TXP7 C599
U36 C PEG TXP8 C605
U39 C PEG TXP9 C602
Y39 C PEG TXP10 C609
Y46 C PEG TXP11 C595
AA36 C PEG TXP12 C617
AA39 C PEG TXP13 C620
AD42 C PEG TXP14 C615
AD46 C PEG TXP15 C592

IV&EV Dis/Enable setting

<5/31>Montevina_Schematics_Checklist_Rev0.8

a) For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But
design guide Rev0.7 show NC. What is correct.
b) For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA,
CRT_HSYNC, CRT_VSYNC. These signals should be connected to
GND. But design guide Rev0.7 show NC, Intel suggest follow
Design guide.

<check list>

For EV@

CRT R/G/B 0ohm to GND CRT R/G/B 150ohm to GND
CRTIREF 0ohm to GND CRTIREF 1Kohm to GND

For topology without the analog switch
- if the total motherboard route
length is less than 12", the
recommended reference
resistor value is 1 kΩ ±1%

CRTIREF
For IV: 1Kohm
For EV:0ohm



SP@

CRT R/G/B
For IV: 150ohm
For EV:0ohm

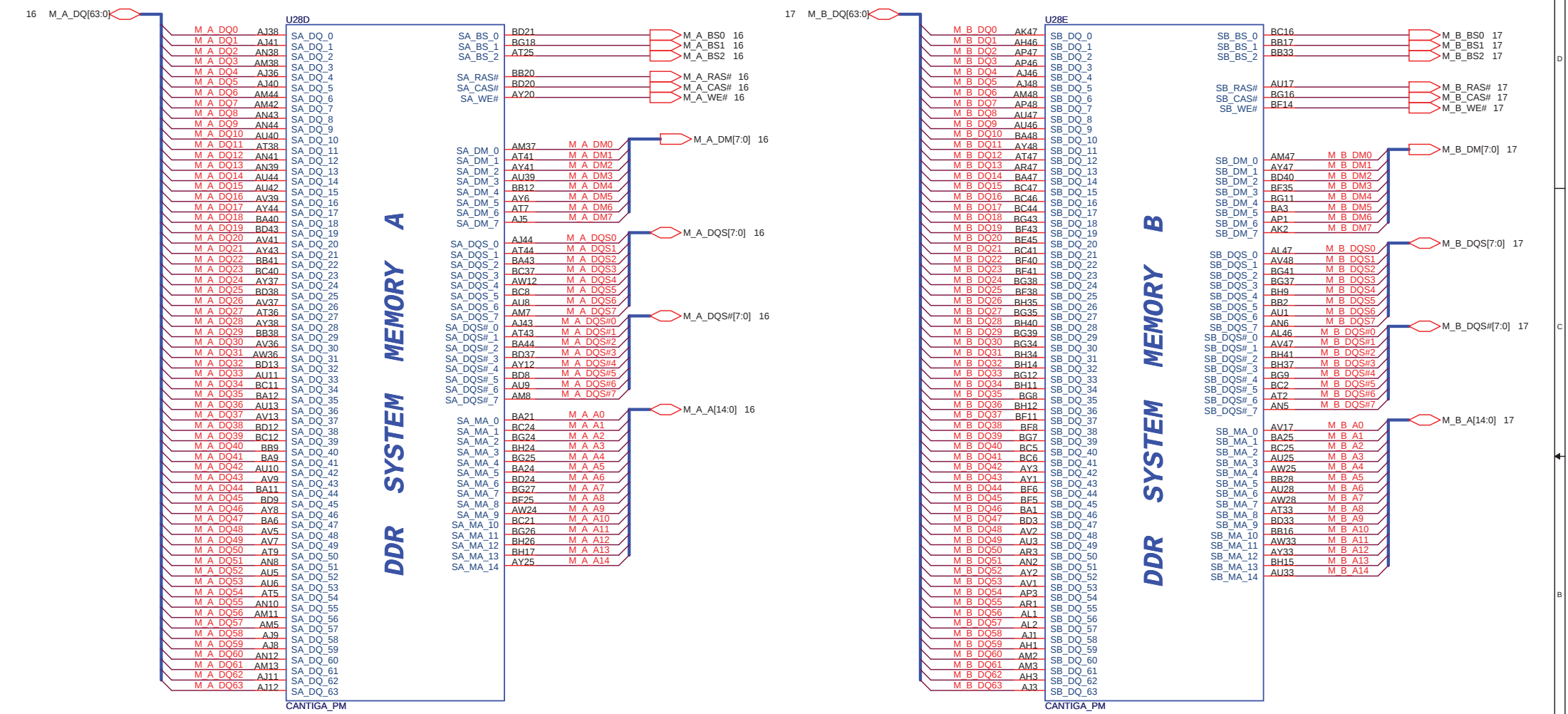


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GMCH VGA

GMCH-CANTIGA(CLG)



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GMCH VCC,NCTF		
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Power consumption reference to Intel Cantiga chipset EDS Volume1. Section 10

External Graphics (GMCH Integrated Graphics Disable)

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCB_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TV_DAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

IV@
EV@
SP@

1210 10uH, 10%
0.45A DCR_max = 0.39

1.05V
64.8mA for DPLL A/B

1210 10uH, 10%
0.45A DCR_max = 0.39

ESR=15 m

1210 0.1uH, 20%, 1A,
DCR_max=0.078Ω

ESR=15 m

3.3V
24.15mA for VCCA_TV_DAC
39.48mA for VCCA_TV_DAC
24.15mA for VCCA_TV_DAC
Total 87.78mA

FB 180@100 MHz, 25% 1.5A
DCR_max=90 m

CRB no 10U
Check list need min 10U-100U for VCCA_TV_DAC

VCCD_TV_DAC always keep 0.1u/0.022u/10u to +1.5V

1.5V
48.363mA for CRT
5mA for TV

FB 220@100 MHz, 25%, 2A

ESR=60m ohm

If CRT have Flicker issue
STUFF 5.6 ohm

IV&EV Dis/Enable setting

IV&EV Dis/Enable setting

SP@:INT use 0.1u
EXT use 0 ohm

VCCA_DPLLA/B always keep to +1.05V
(if no use IV dynamic core power)

USE same GND plane

1.8V
13.2mA

1.05V
50mA

1.05V
139.2mA

1.05V
50mA

1.05V
50mA

1.5V
50mA

1.5V
35mA

1.5V
157.2mA

1.5V
0.5mA

1.05V
50mA

1.05V
50mA

1.8V
60.31mA

IV&EV Dis/Enable setting

SP@:INT use 1 U
EXT use 0 ohm

3.3V
73mA

3.3V
5mA

1.05V DPLLA

1.05V DPLLB

1.05V HPLL

1.05V MPLL

1.8V TXLVDS

VCCA_LVDS

VSSA_LVDS

VCCA_PEG_BG

VCCA_PEG_PLL

VCCA_PEG_PLL

VCCA_PEG_PLL

VCCA_PEG_PLL

VCCA_PEG_PLL

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VCCA_PEG_PLL

3.3V
73mA

3.3V
5mA

1.05V DPLLA

1.05V DPLLB

1.05V HPLL

1.05V MPLL

1.8V TXLVDS

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3.3V
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1.05V DPLLB

1.05V HPLL

1.05V MPLL

1.8V TXLVDS

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1.05V DPLLB

1.05V HPLL

1.05V MPLL

1.8V TXLVDS

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VSSA_LVDS

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3.3V
73mA

3.3V
5mA

1.05V DPLLA

1.05V DPLLB

1.05V HPLL

1.05V MPLL

1.8V TXLVDS

VCCA_LVDS

VSSA_LVDS

VCCA_PEG_BG

VCCA_PEG_PLL

VCCA_PEG_PLL

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VCCA_PEG_PLL

VCCA_PEG_PLL

VCCA_PEG_PLL

3.3V
73mA

3.3V
5mA

1.05V DPLLA

1.05V DPLLB

1.05V HPLL

1.05V MPLL

1.8V TXLVDS

VCCA_LVDS

VSSA_LVDS

VCCA_PEG_BG

VCCA_PEG_PLL

VCCA_PEG_PLL

VCCA_PEG_PLL

VCCA_PEG_PLL

VCCA_PEG_PLL

VCCA_PEG_PLL

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VCCA_PEG_PLL

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VCCA_PEG_PLL

VCCA_PEG_PLL

VCCA_PEG_PLL

VCCA_PEG_PLL

VCCA_PEG_PLL

3.3V
73mA

3.3V
5mA

1.05V DPLLA

1.05V DPLLB

1.05V HPLL

1.05V MPLL

1.8V TXLVDS

VCCA_LVDS

VSSA_LVDS

VCCA_PEG_BG

VCCA_PEG_PLL

VCCA_PEG_PLL

VCCA_PEG_PLL

VCCA_PEG_PLL

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VCCA_PEG_PLL

VCCA_PEG_PLL

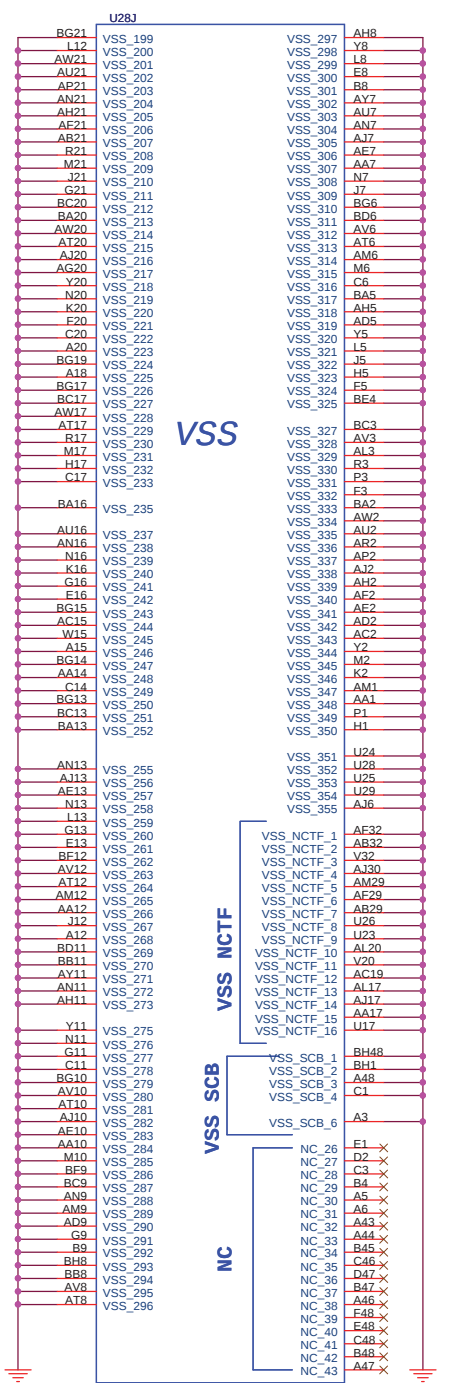
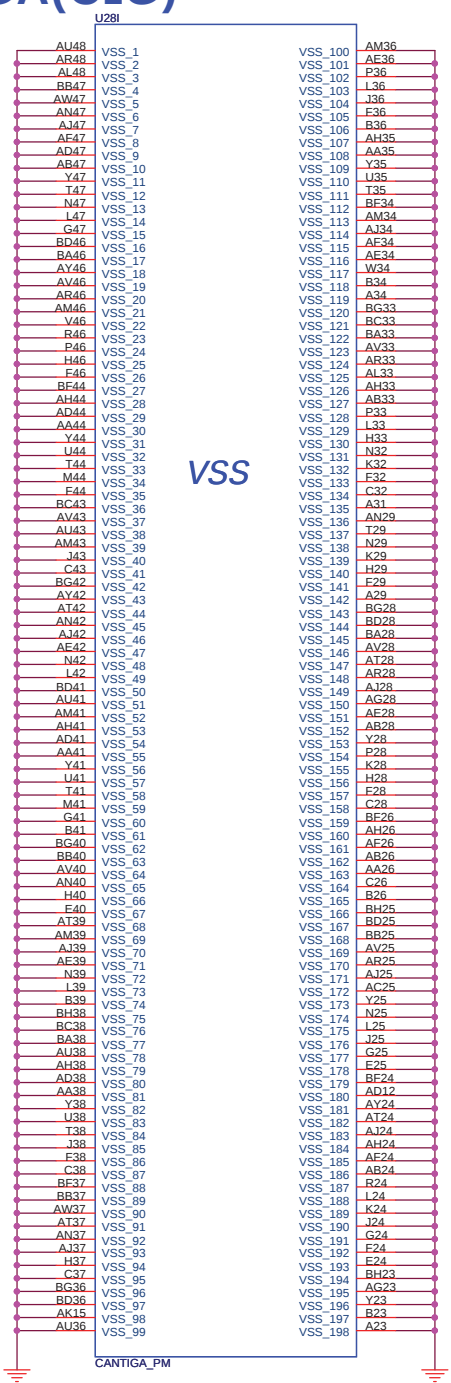
VCCA_PEG_PLL

VCCA_PEG_PLL

VCCA_PEG_PLL

VCCA_PEG_PLL

GMCH-CANTIGA(CLG)





Quanta Computer Inc.

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GMCH VSS

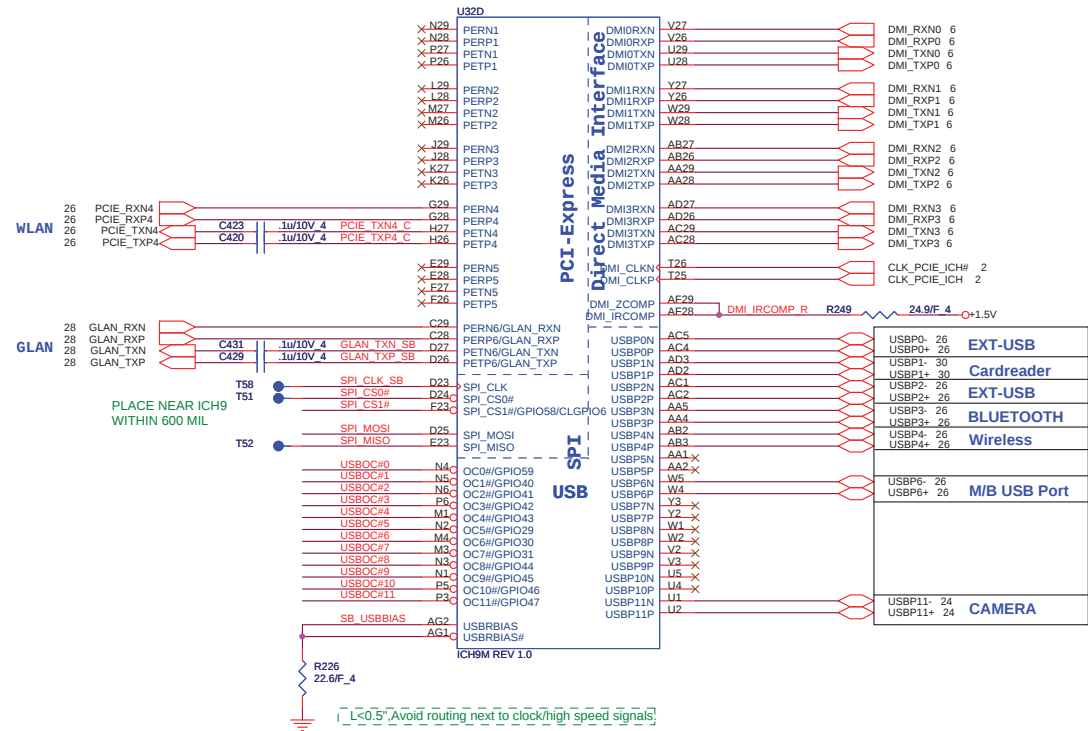


The schematic diagram illustrates the HDA pin connections for the Intel Atom D4015. It shows the following components and connections:

- HDA_SDOUR_R:** Connected to MXM_SDOUR_HDMI (21), HDA_SDOUR_HDMI (6), and ACZ_SDOUR_AUDIO (27). It includes resistors R225, R216, and R221, and a voltage divider *EV@33_4. A note indicates "Weak integrated PD on the HDA_SDOUR pin." A capacitor C357 (*10p/50V_4) is connected to ground.
- HDA_SYNC_R:** Connected to MXM_SYNC_HDMI (21), HDA_SYNC_HDMI (6), and ACZ_SYNC_AUDIO (27). It includes resistors R241, R220, and R224, and a voltage divider *EV@33_4. A note indicates "Weak integrated PD on the HDA_SYNC pins." A capacitor C361 (*10p/50V_4) is connected to ground.
- HDA_BIT_CLK_R:** Connected to MXM_BIT_CLK_HDMI (21), HDA_BIT_CLK_HDMI (6), and BIT_CLK_AUDIO (27). It includes resistors R219, R215, and R239, and a voltage divider *IV@33_4. A note indicates "24.000 MHz is output from the [CH9M]." A central box labeled "For EMI" shows a series combination of capacitor C362 (*10p/50V_4) and resistor R223 (*22_4) connected to HDA_BIT_CLK_R. Capacitors C369, C353, and C360 (*10p/50V_4) are connected to ground.
- HDA_RST#_R:** Connected to MXM_RST#_HDMI (21), HDA_RST#_HDMI (6), and ACZ_RST#_AUDIO (27). It includes resistors R213, R214, and R253, and a voltage divider *EV@33_4.
- HDA_SDIN3 and HDA_SDIN2:** Connected to MXM_SDIN_HDMI (21) and HDA_SDIN_HDMI (21). They include resistors R228 and R227, and a voltage divider *IV@0_4.

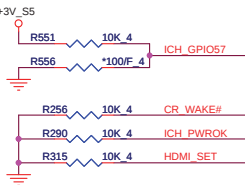
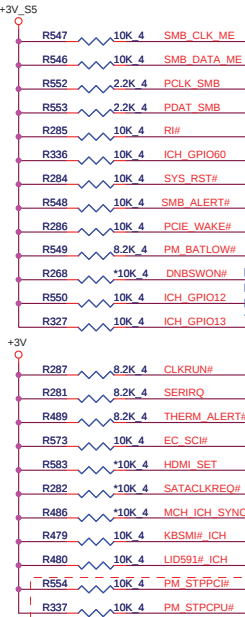
[illegible]

Pin Name	Strap description	Sampled	Configuration			PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect			This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU			
TP3	XOR Chain Entrance	PWROK	ICH_TP3	HDA_SDOUT	Description	
			0	0	RSVD	
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	0	1	Enter XOR Chain	
			1	0	Normal operation(Default)	
			1	1	Set PCIE port config bit 1	



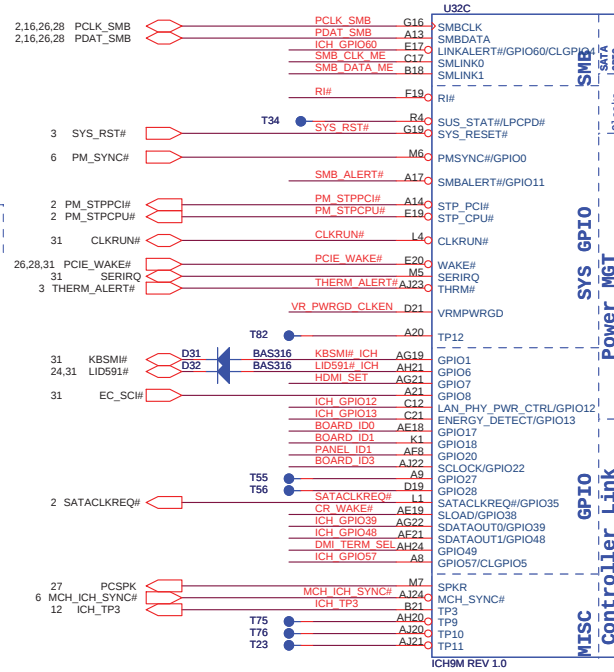
Pin Name	Strap description	Sampled	Configuration			PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0			
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default			
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default			
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default			
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable			
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0	SPI_CS#1	Boot Location	
			0	1	SPI	
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1	0	PCI	
			1	1	LPC(Default)	

ICH9M(CLG)

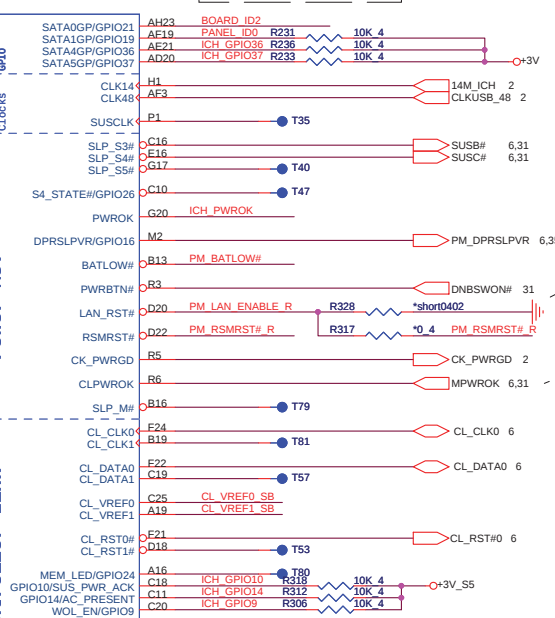


TPM Physical Presence for iTPM.	
Stuff	HDMI SET
R583	HDMI
R315	No HDMI

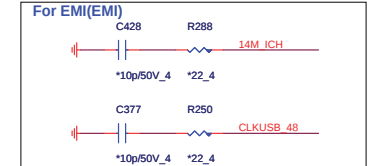
Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)



SATA[x]GP pins if unused require
8.2-k to 10-k pull-up to Vcc3_3 or
8.2-k to 10-k pull-down to ground



ZS2 Default not
 support IAMT. So this
 interface follow
 CRB/Checklist PU
 only

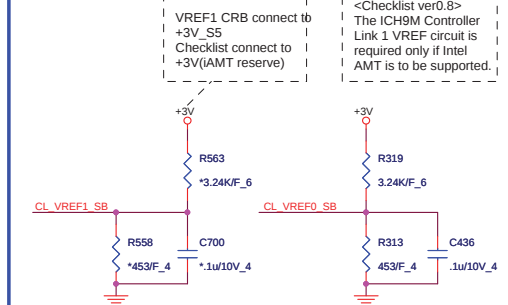


I <Checklist ver0.8>

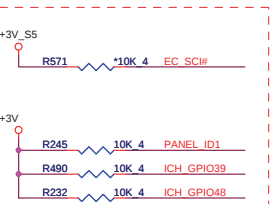
If Intel LAN is used with Wake On LAN, tie LAN_RST# to RSMRST# and NC 0ohm.

CL_PWROK must not assert after PWROK asserts for IAMT.
CL_PWROK to the NB and SB should be connected to existing PWROK inputs on the NB and SB on a platform with no IAMT

CL VREF

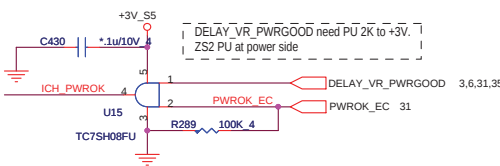


<Checklist ver0.8>
The ICH9M Controller
Link 1 VREF circuit is
required only if Intel
AMT is to be supported.

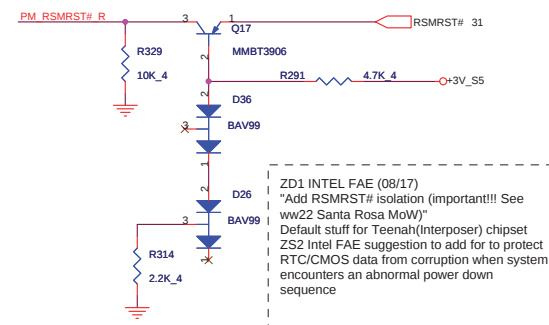


Follow CHECK LIST V1.5

ICH PWROK

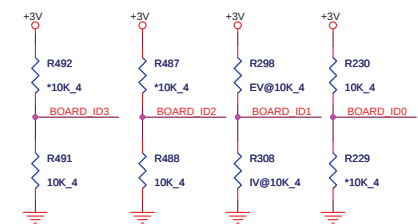


Resume RST



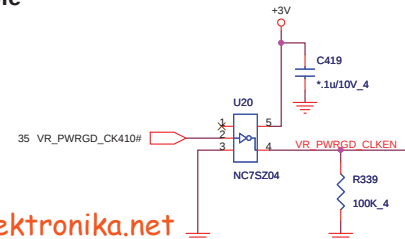
ZD1 INTEL FAE (08/17)
 "Add RSMRST# isolation (important!!! See
 ww22 Santa Rosa MoW)"
 Default stuff for Teenah(Interposer) chipset
 ZS2 Intel FAE suggestion to add for to protect
 RTC/CMOS data from corruption when system
 encounters an abnormal power down
 sequence

M/B ID ID0=0 -->ZK6 , ID0=1 -->ZR6
ID1=0 -->UMA , ID1=1 -->Discrete



Board ID	ID3	ID2	ID1	ID0
A-SMT,ID1=0 -->UMA ,ID1=1 -->Discrete	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1

CLK Enable

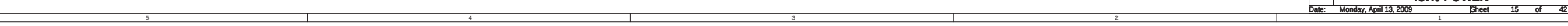


South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	

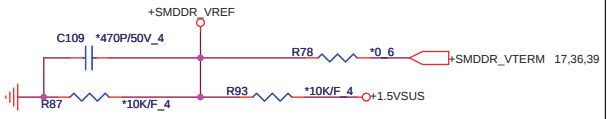
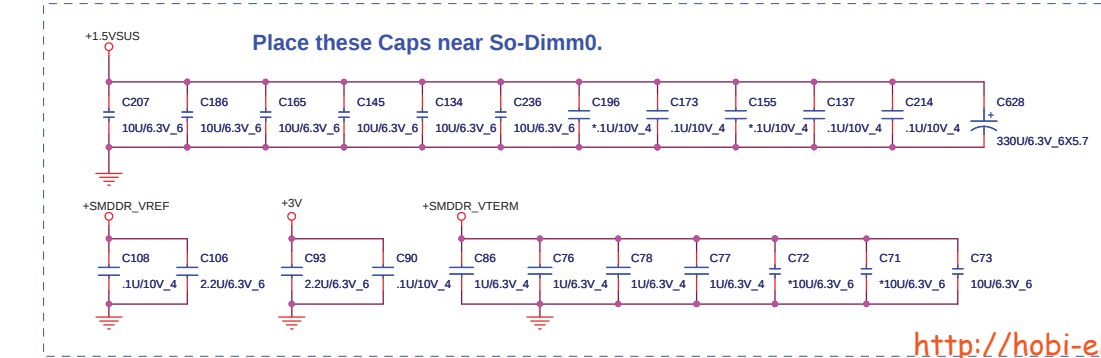
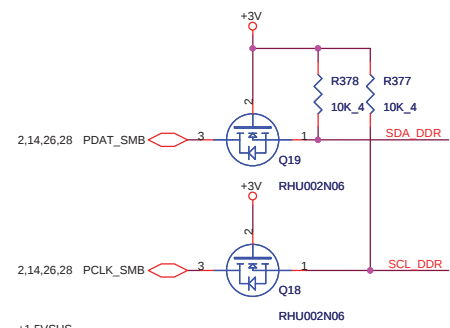
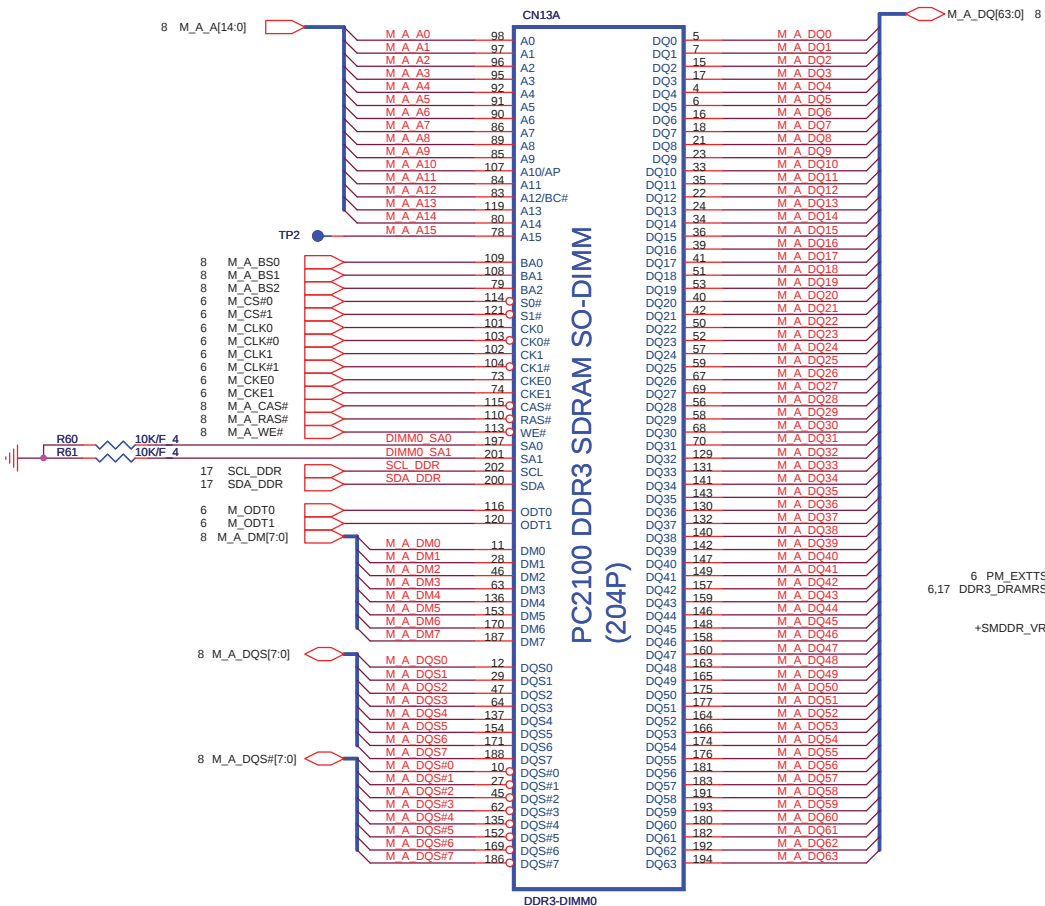
<http://hobi-elektronika.net>

5

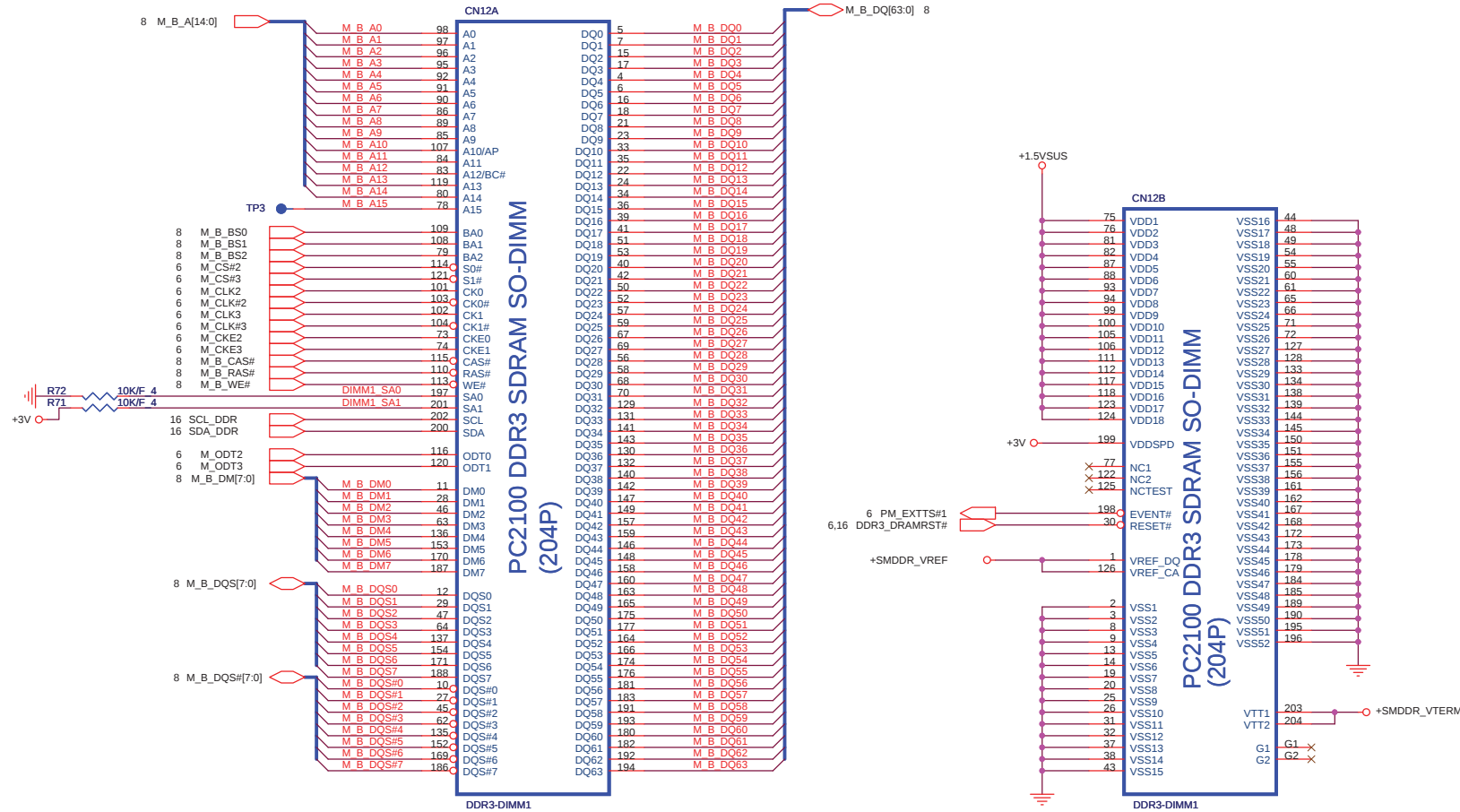


DDR3 (DDR)

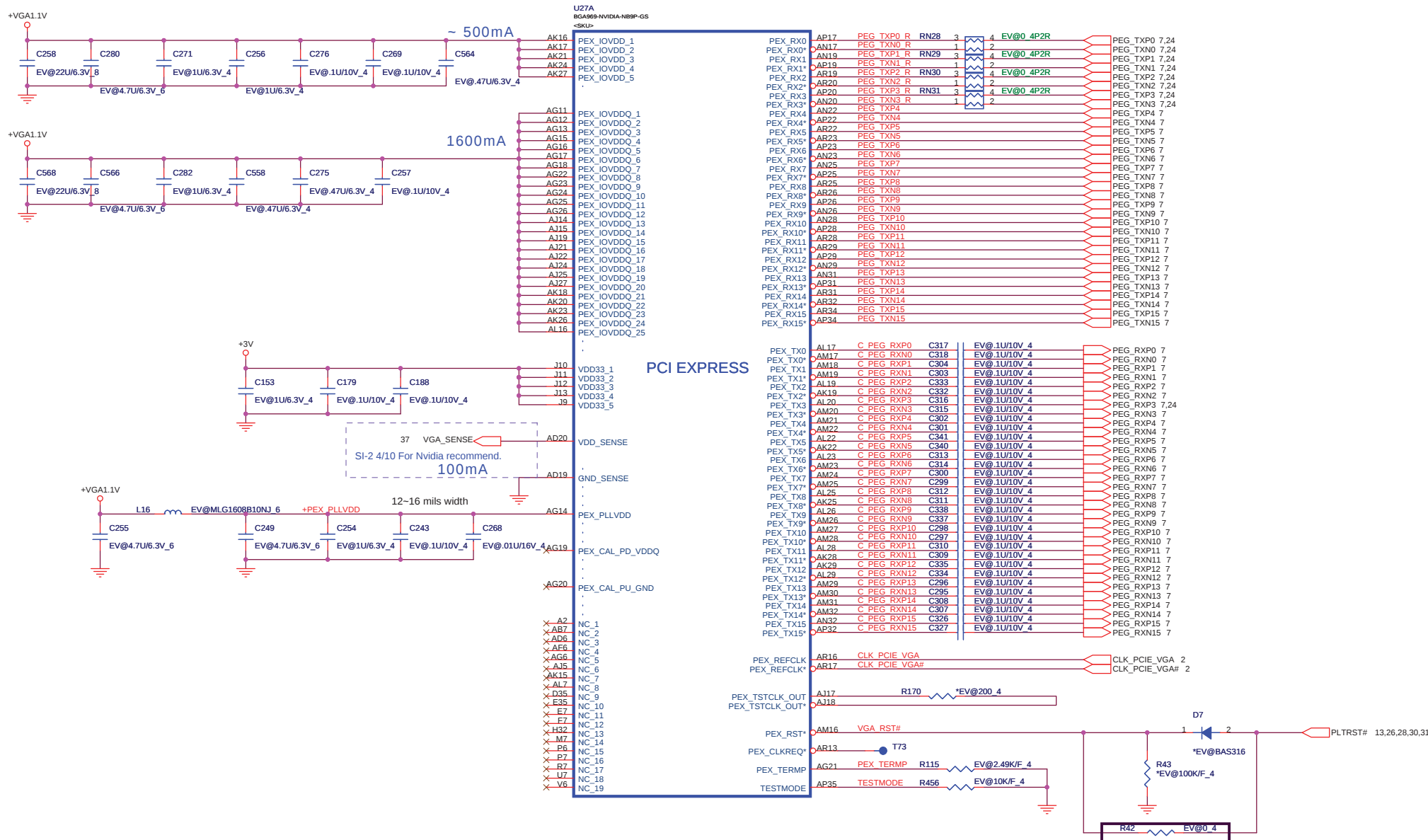
16

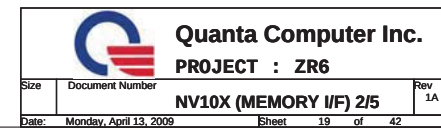


<http://hobi-elektronika.net>



<http://hobi-elektronika.net>

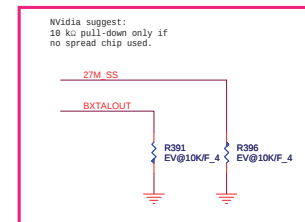


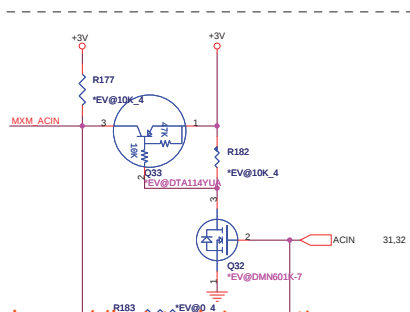
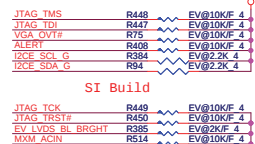


Display port output

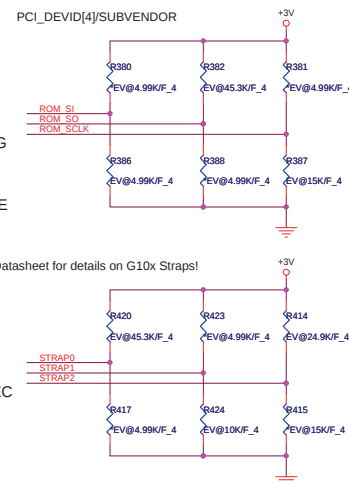
SI Build

27M_NONSS



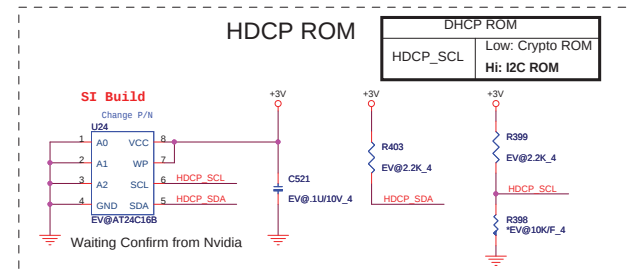


GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

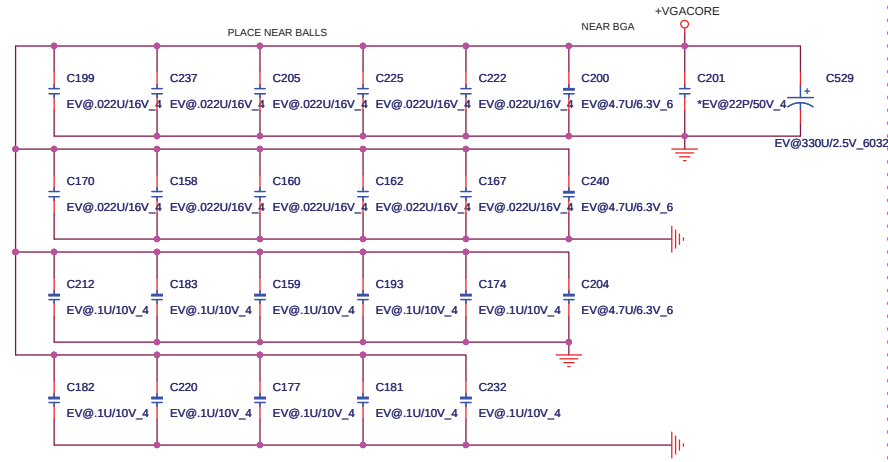
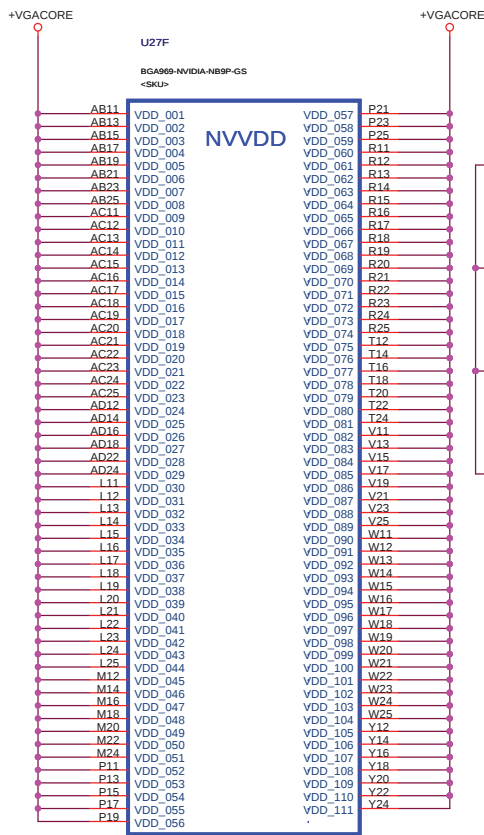


			Logical Strap Bit Mapping		
			R#14	PU-VDD	PD
PCI_DEVID: STRAP2					
NB9M-GE	0x06E	8 1000	5K	1000	0000
NB9M-GS	0x06E	9 1001	10K	1001	0001
NB9P-GE2	0x064	8 1000	15K	1010	0010
NB9P-GS	0x064	9 1001	20K	1011	0011
N10P-GE1	0x065	2 0010	25K	1100	0100
N10M-GE1	0x06E	C 1100 default	30K	1101	0101
			35K	1110	0110
			45K	1111	0111

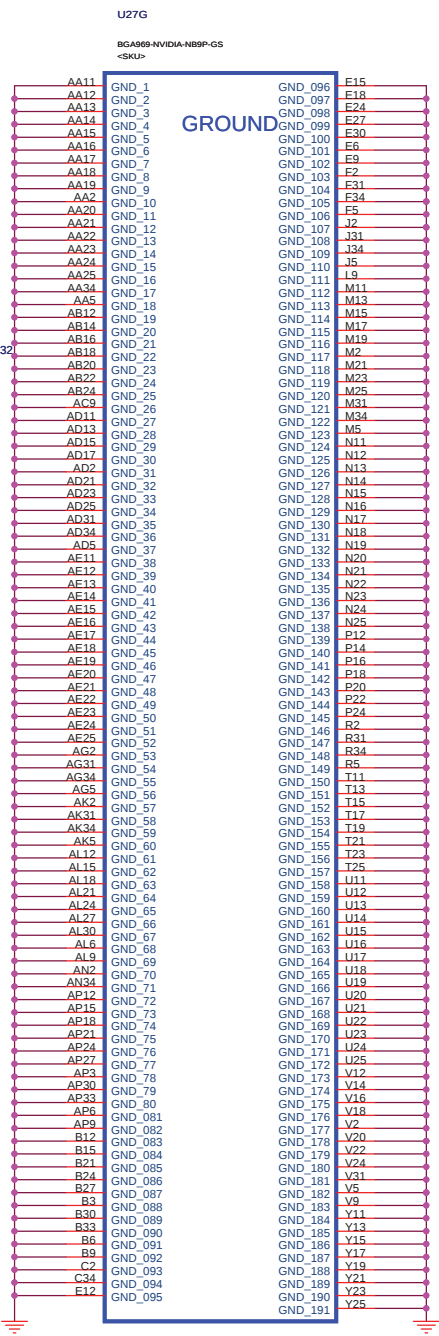
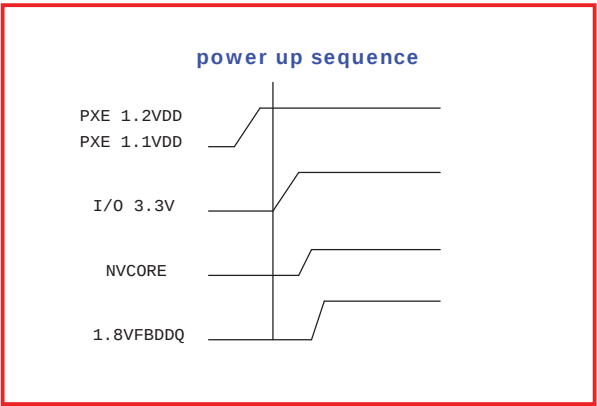
R386	Config	Definitions	Die
CS25102FB02 5K	64Mx16 DDR2	Hynix	E
CS31002FB26 10K	64Mx16 DDR2	Samsung	Q
CS32002FB29 20K	64Mx16 DDR2	Samsung	E



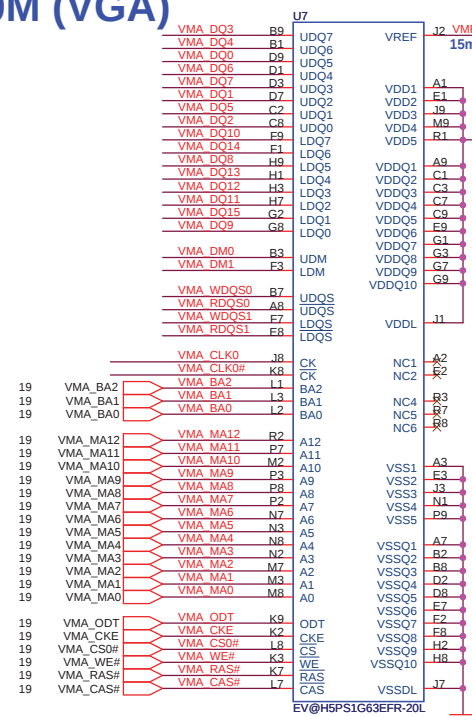
NVVDD Decoupling



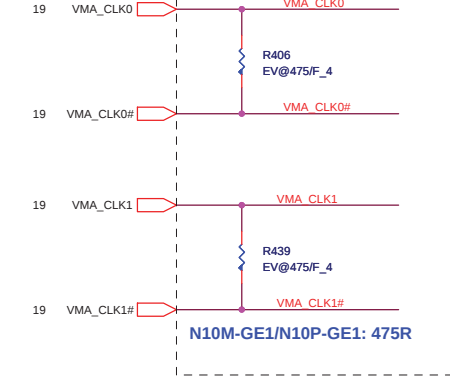
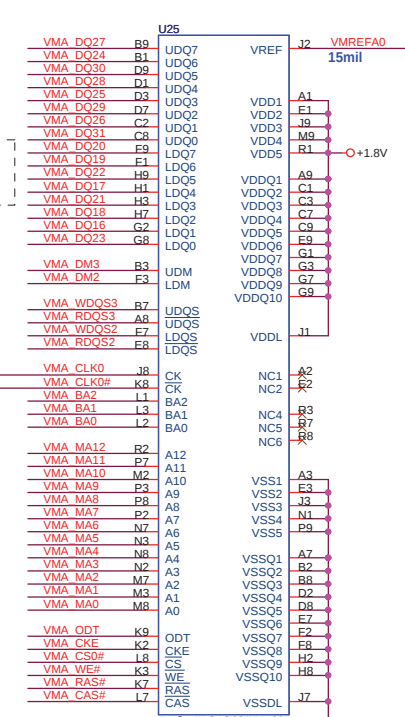
Follow Design Guide DG-03276-001 4.7uF x3 and 0.22x10 uF instead of 0.1uF x10



NV10M (VGA)

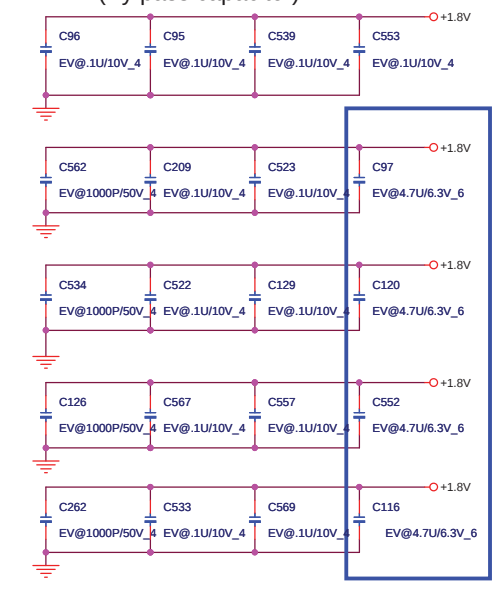


SI Build
N10P-GE1/N10M-GE1: 50% FBVDD
N10M-GE1: 50% ,R429 (1K)



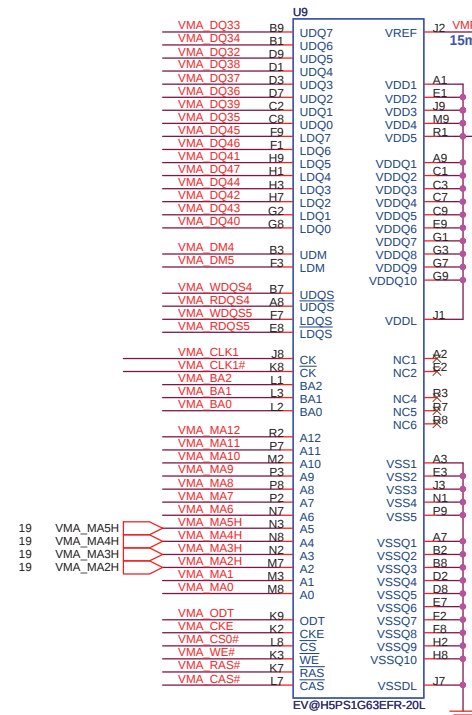
CS14752FB11 RES CHIP 475 1/16W +-1%(0402)

(By pass capacitor)

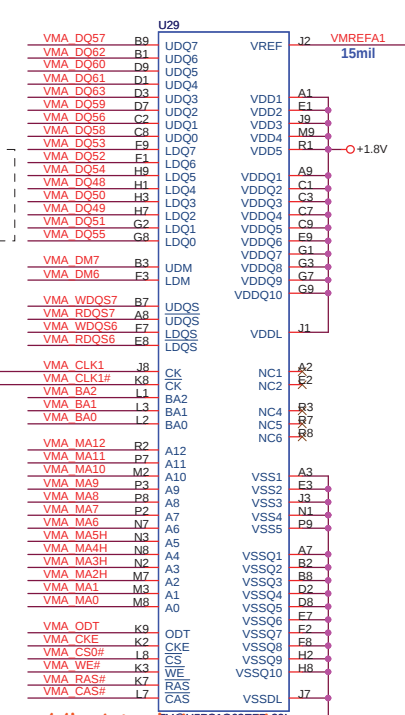


For DB:
N10P/N10M : AKD5LG-T510(Samsung,64M*16)
AKD5LG-TW02(Hynix,64M*16)

- 19 VMA_DQ[63..0]
- 19 VMA_DM[7..0]
- 19 VMA_WDQS[7..0]
- 19 VMA_RDQS[7..0]

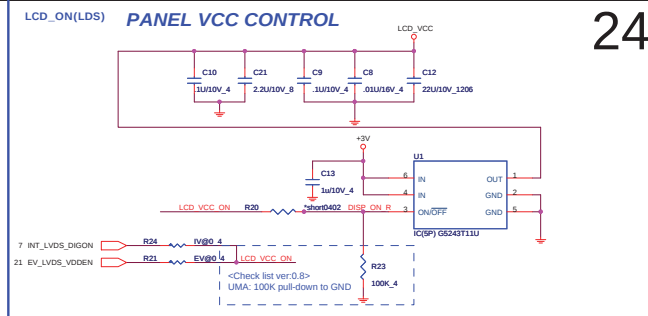


SI Build
N10P-GE1/N10M-GE1: 50% FBVDD
N10M-GE1: 50% ,R433 (1K)

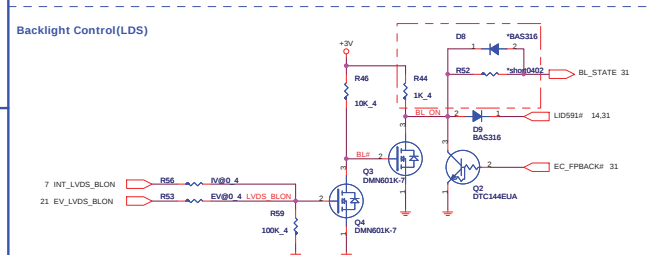


<http://hobi-elektronika.net>

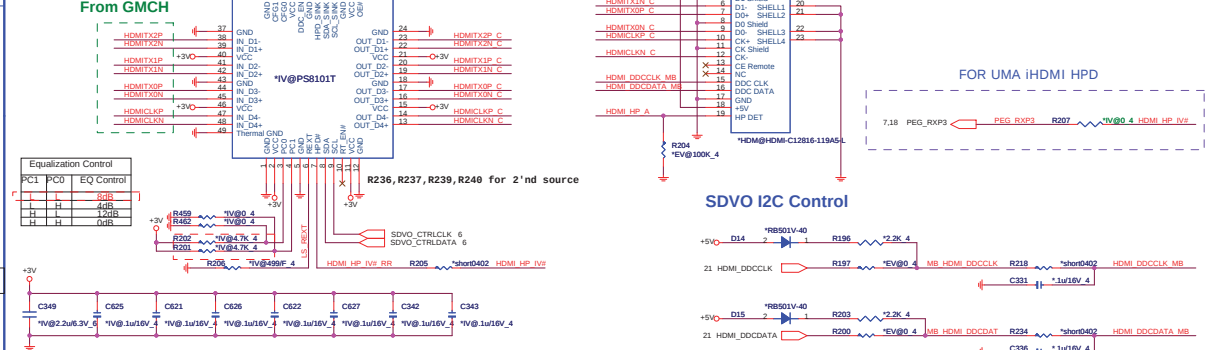
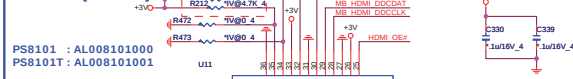
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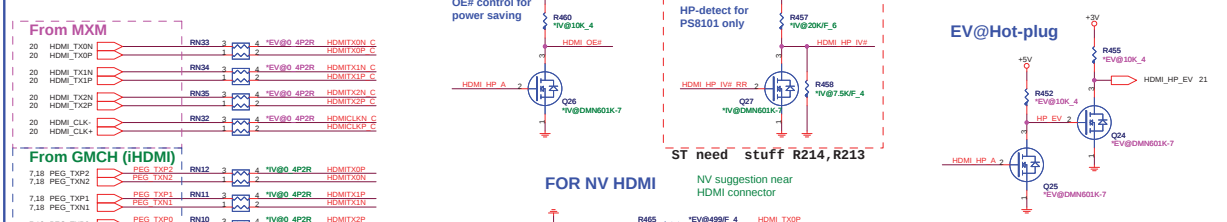
Backlight Control(LDS



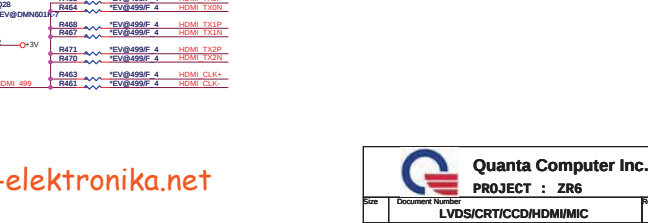
HDMI (HDM)



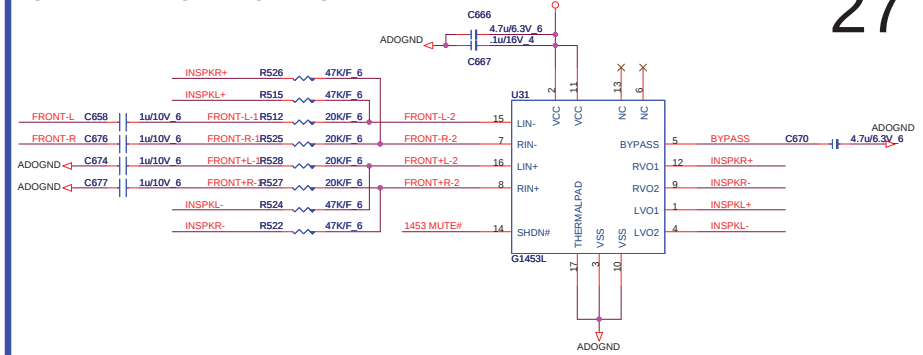
100



Modify

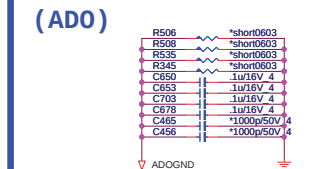


27



The schematic diagram illustrates the HPPLG# signal path. It starts with HPL and HPR inputs, which are filtered by 5.1k resistors (R530, R533) and 150nH inductors (L49, L50). The resulting HPL_SYS and HPR_SYS signals pass through 1k resistors (R534, R531) and a 100pF/50V capacitor (C682). The signal then passes through another 100pF/50V capacitor (C672) and a 10k resistor (R539) to the HPPLG# pin of the DMN601K-7 component. The HPPLG# pin is also connected to the Line-in JACK Green connector (CN21) and the 3AVDD pin. The signal path is terminated at ADOGND.

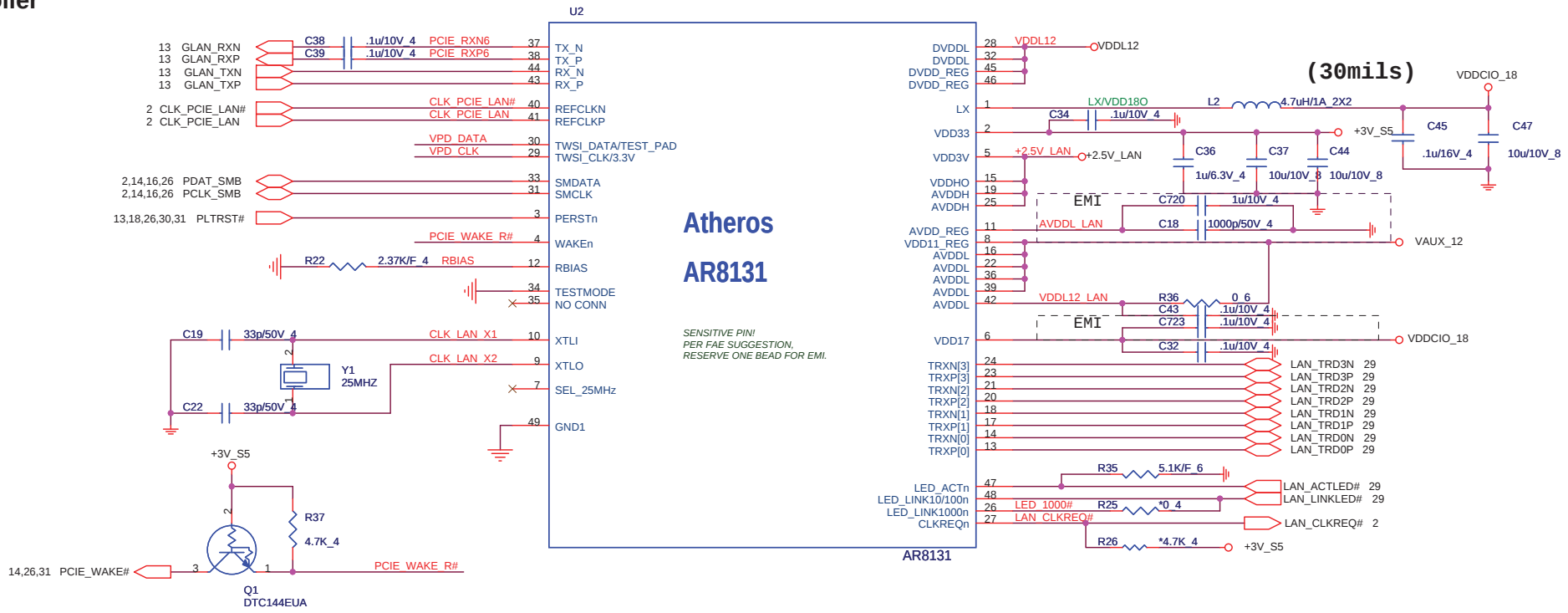
The schematic shows the input of an AND gate. A red wire labeled "AND_MUFFIN" connects pin 1 of the gate to a +3V supply through a resistor R564 (100K_4). Pin 2 of the gate is connected to a network of capacitors: C598 (1uF16V_4), C703 (1uF16V_4), C678 (1uF16V_4), C465 (*1000p50V_4), and C456 (*1000p50V_4). The other ends of these capacitors are connected to a common node labeled ADOGND.



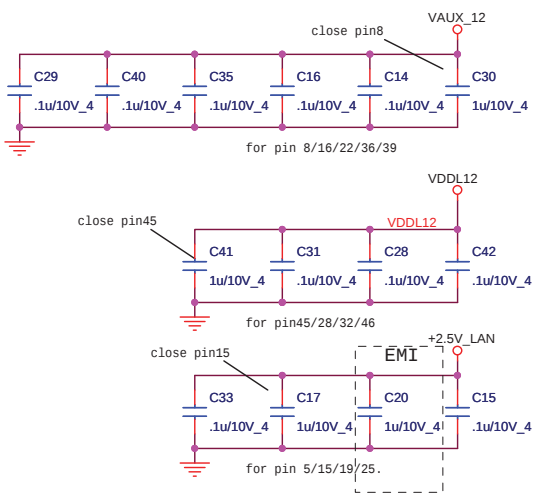
 **Quanta Computer Inc.**
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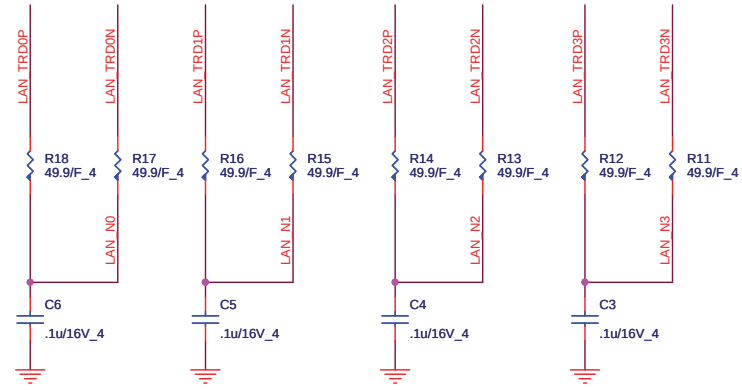
LAN Controller



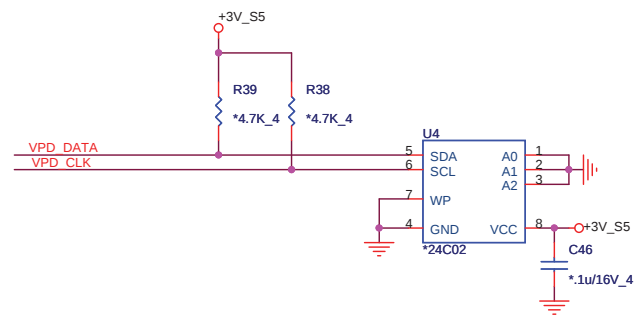
Decoupling CAP



PLACE NEAR IC SIDE



EEPROM

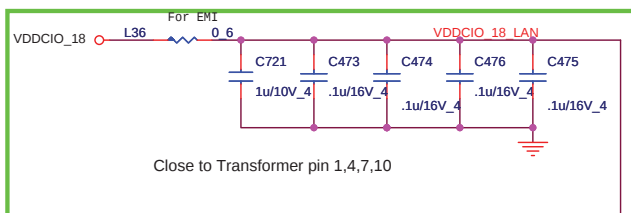


Quanta Computer Inc.

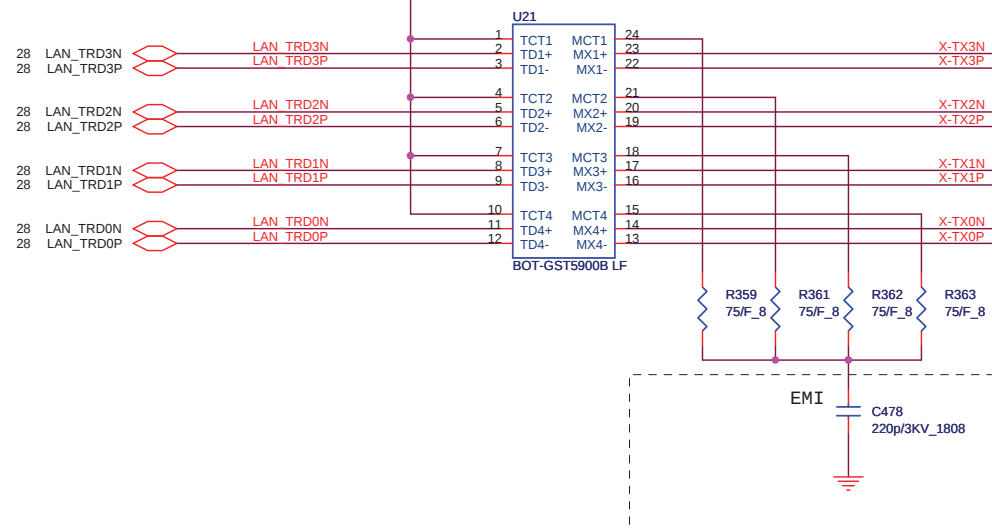
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AR8131 GLAN

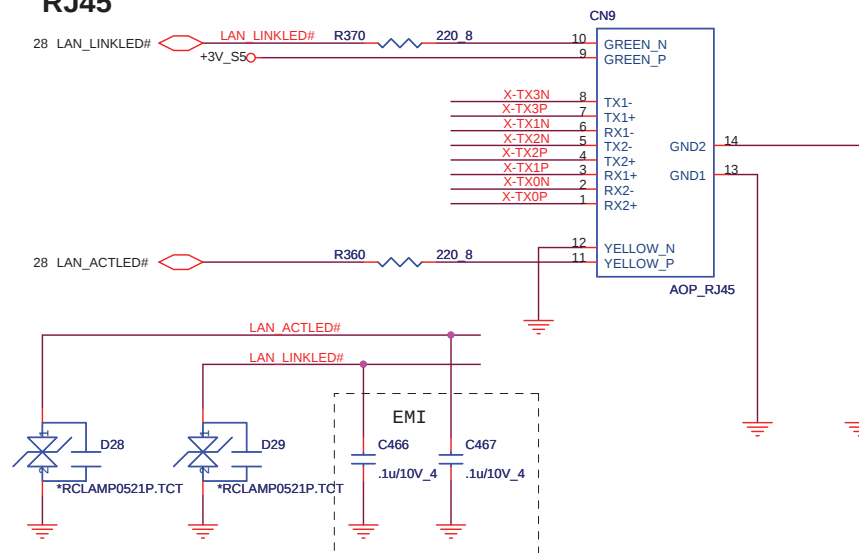
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TRANSFORMER



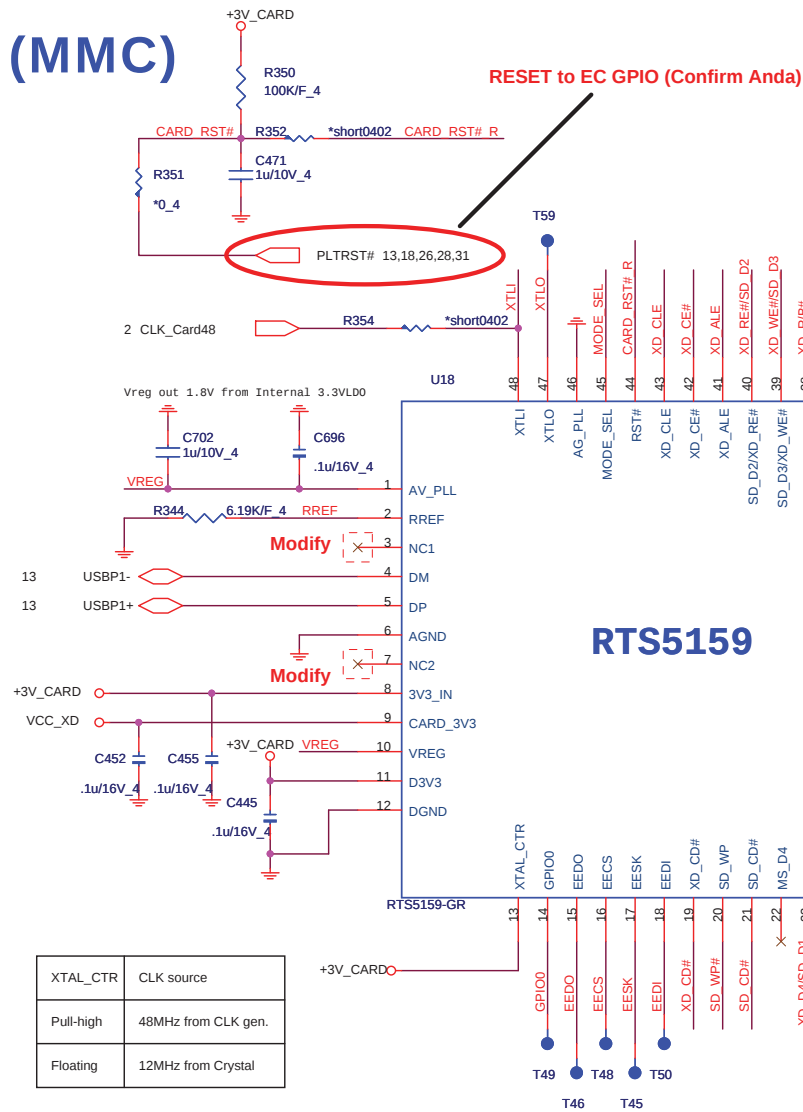
RJ45

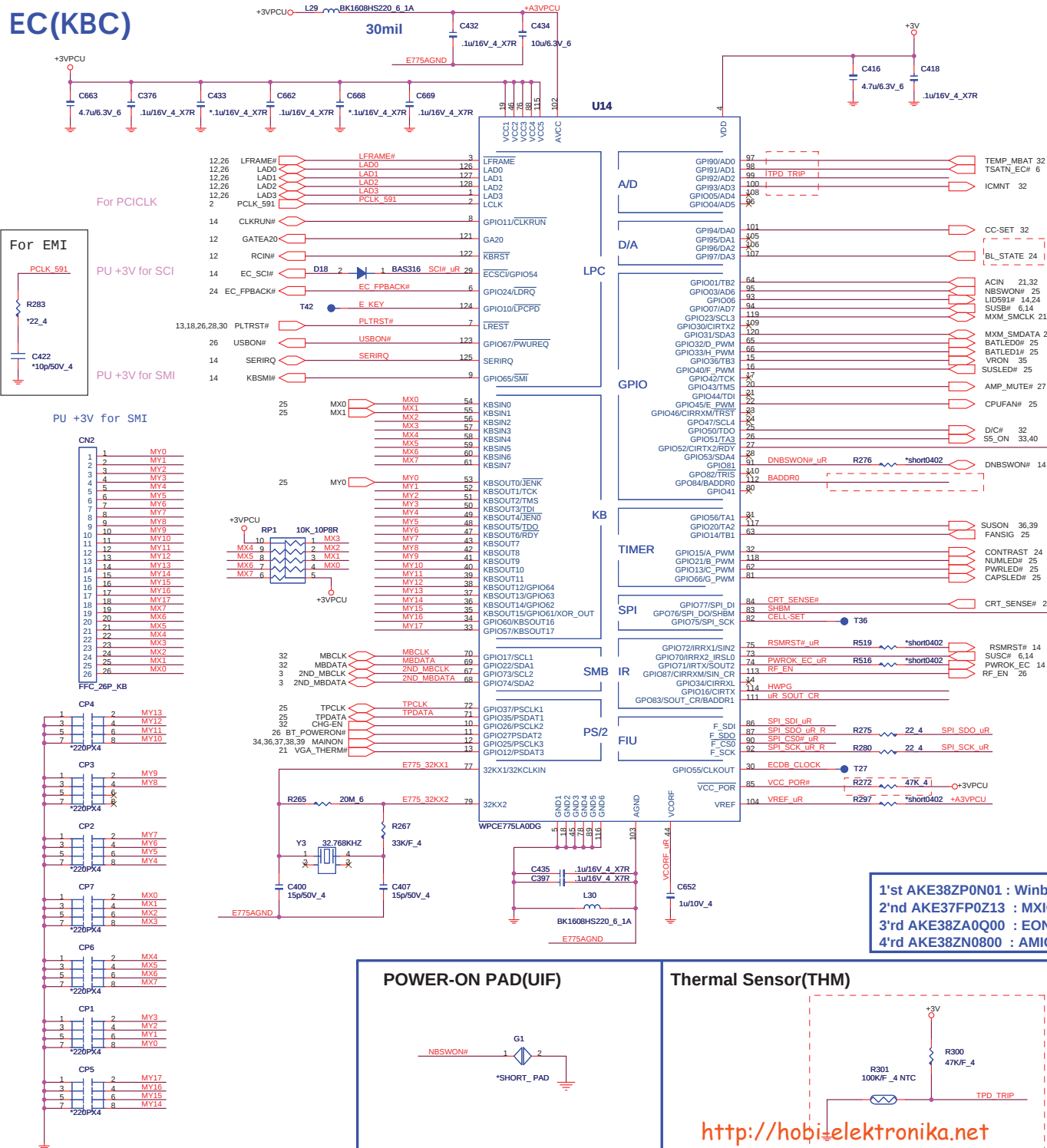


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(MMC)

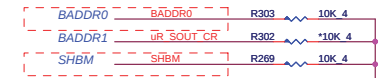




I/O ADDRESS SETTING

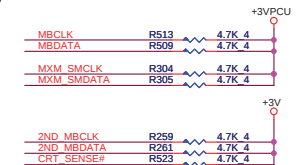
I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

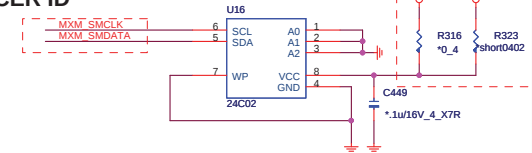


1/13 Confirm by vendor mail :
 Disabled ('1') if using FW device on LPC.
 Enabled ('0') if using SPI flash for both system BIOS and EC firmware

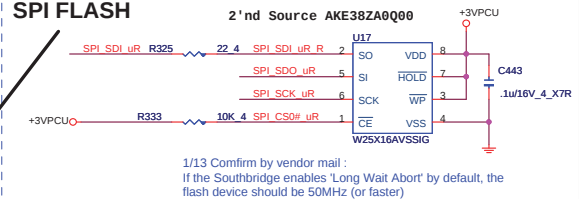
SM BUS PU



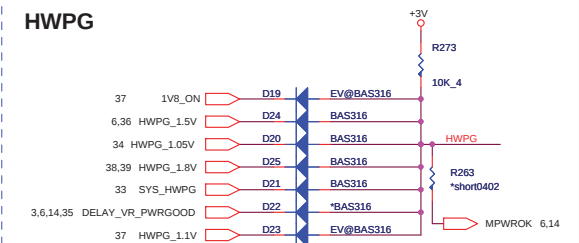
ACER ID



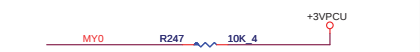
SPI FLASH

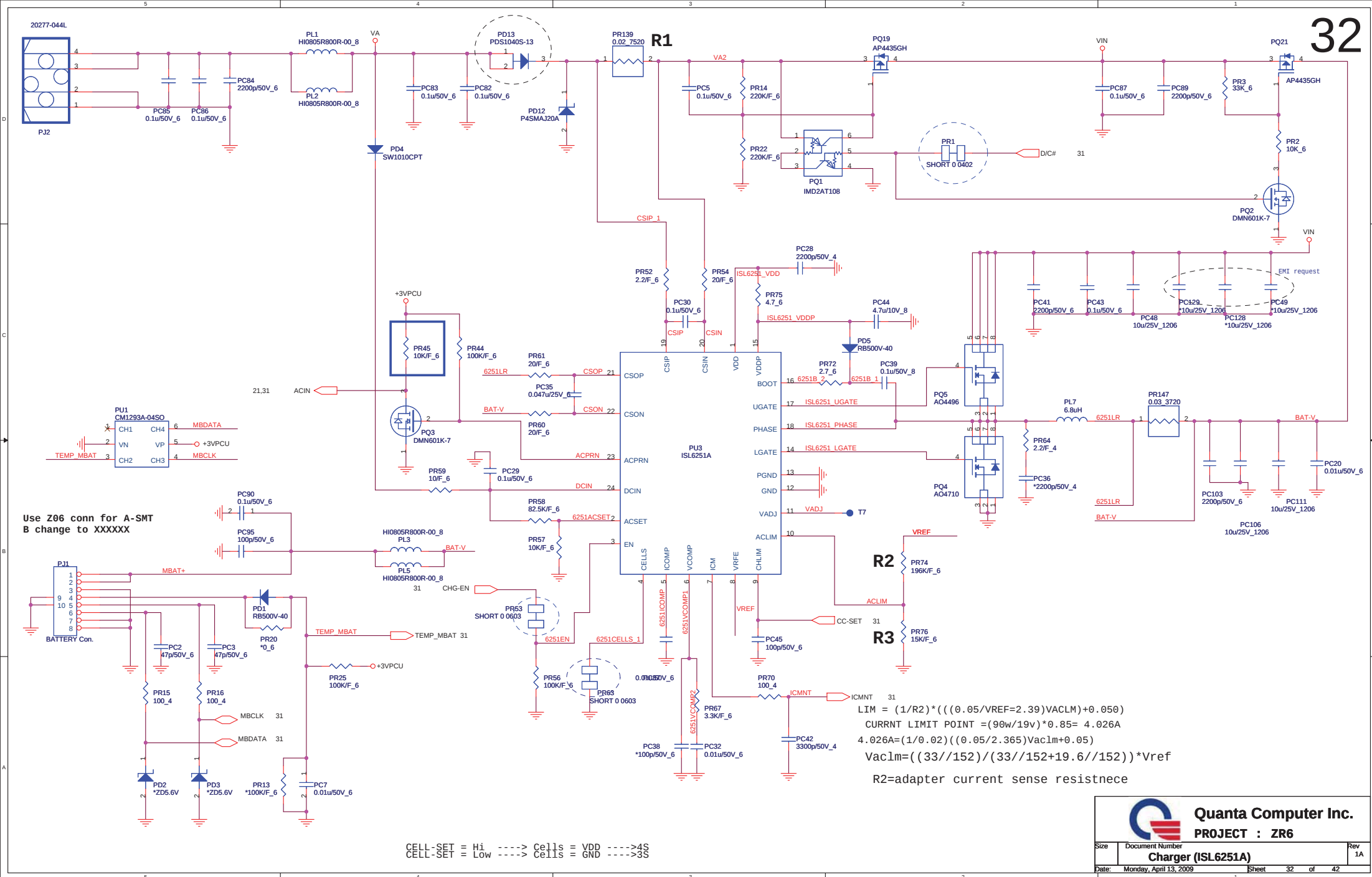


HWPG

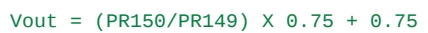


INTERNAL KEYBOARD STRIP SET





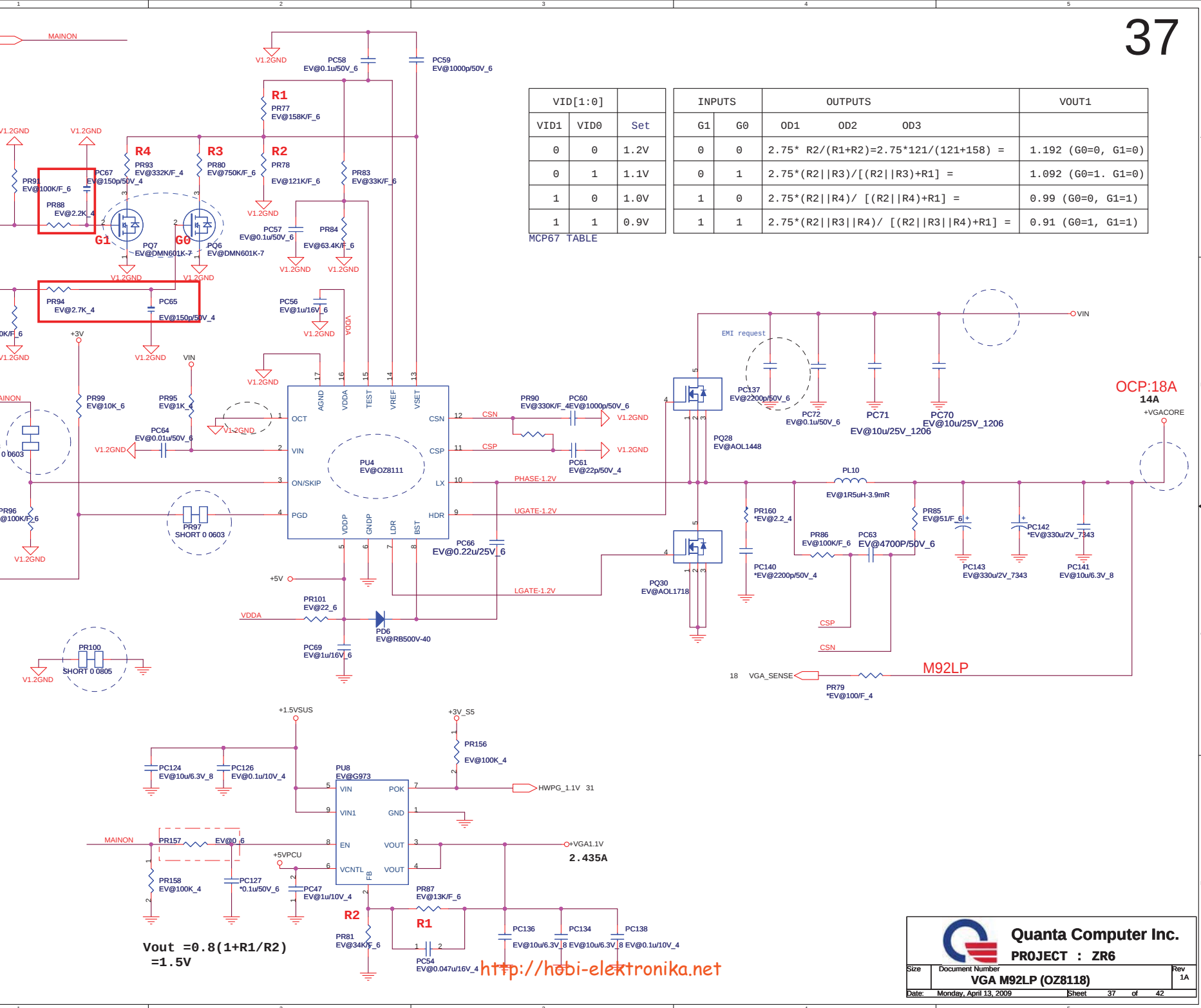



$$OCP = 15.5 + 0.5A$$

4.6m*16=RILIM*10uA

RILIM=5.06K~5.1K

$$(10u \cdot PR154) / Rdson + \Delta I / 2 = I_{ocp}$$

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OCP: 4A

2.73A

$$V_{OUT} = (1 + R1/R2) * 0.75$$

$$R_{ds} * OCP = R_{ILIM} * 20\mu A$$

$$T_{ON} = 3.85p * R_{TON} * V_{out} / (V_{in} - 0.5)$$

$$Frequency = V_{out} / (V_{in} * T_{ON})$$

$$T_{ON} = 3.85p * 1M * 1 / (V_{in} - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

A04932 $R_{ds} = 15.6 \sim 19.6m\Omega$

OCP = 16 - 0.8A

$$L(\text{ripple current}) = (19 - 1.8) * 1.8 / (2.5u * 272k * 19) \sim 2.14A$$

$$19.6m * 4 = R_{ILIM} * 20\mu A$$

$$R_{ILIM} = 3.92K$$

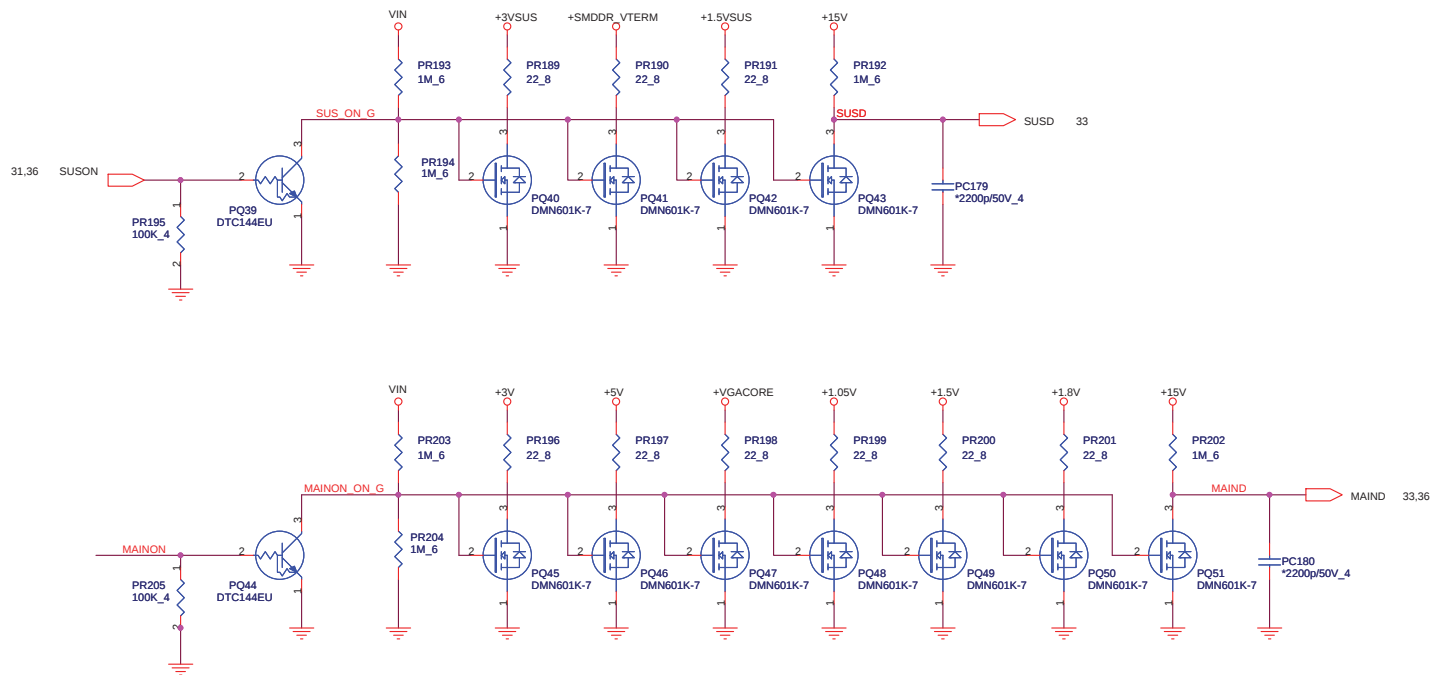
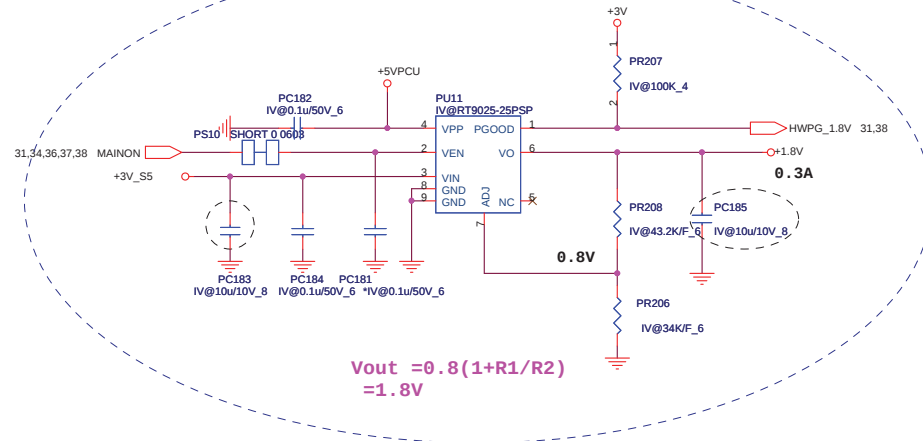


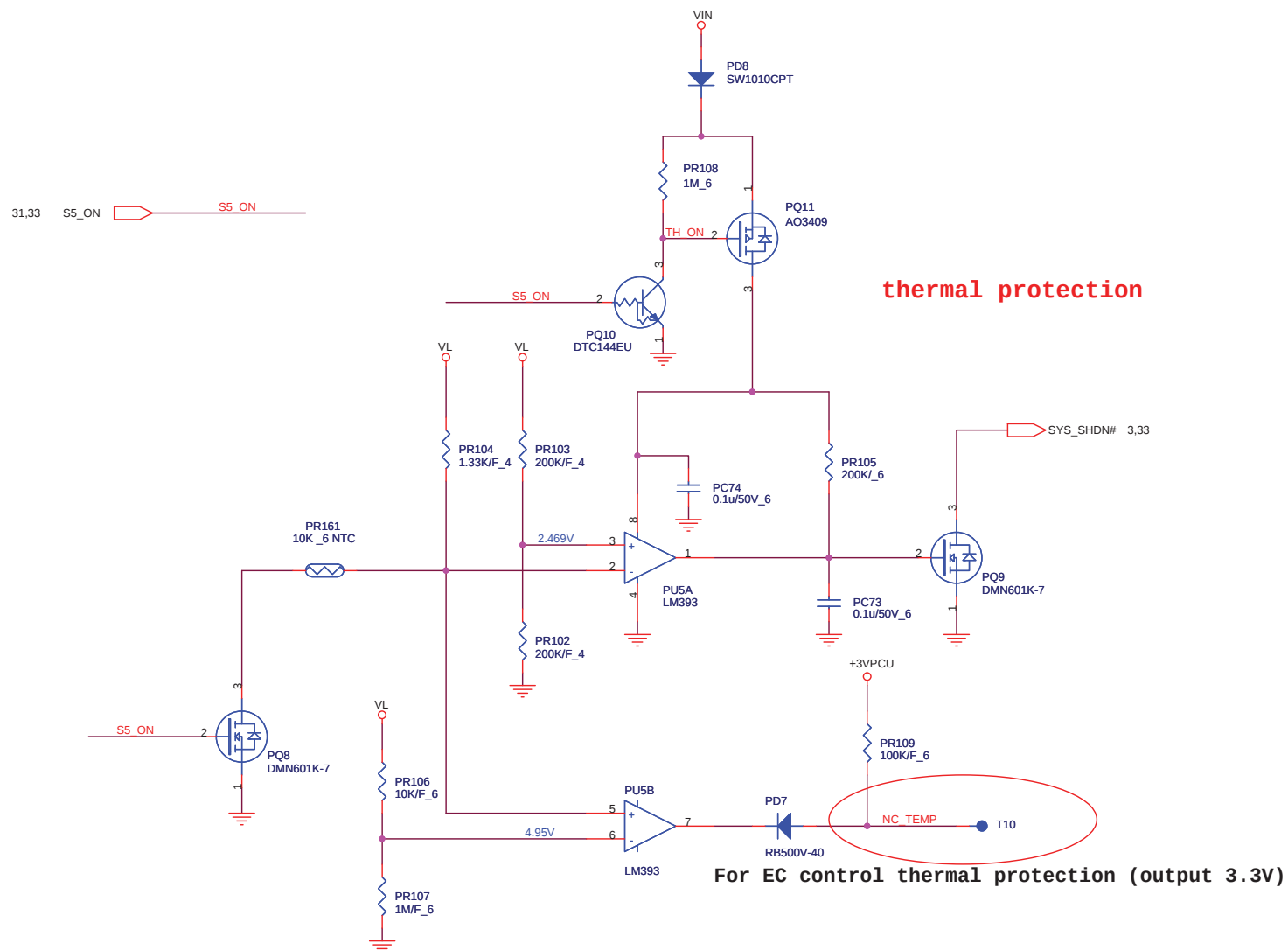
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PROJECT : ZR6

Size	Document Number	Rev
	VCCP 1.8V(UP6111A)	1A

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[illegible]

MODEL: REV		CHANGE LIST		MODEL		ZR6 MB		
				PAGE	FROM	TO		
ZR6 MB	B	Page6:change R175 and R181 to 4.7K for HDMI vender request		1	1A			
	C	Page10:change net name +1.5VSUS_TXLVDS--> +1.8V_TXLVDS		2	1A	3B		
		Page3:Del Q5,Q6,R62,R63		3	1A			
		Page3:change Par Number from AL000780000 to AL000780003 for thermal sensor address change to 9AH		4	1A			
		Page21:Del Q10,Q9,R96,R86		5	2A			
		Page27:R574 stuff and R541 no stuff		6	1A			
		Page31:R300,R301 stuff thermal sensor		7	1A			
		Page37:change PC65,PC67 to 150pF		8	1A			
		Page28:change U2 PartNumber from AL008131001 to AL008131002(LAN chip)		9	3A			
		Page27:change R530,R533 from 10 ohm to 5.1 ohm for headphone		10	3A			
		Page27:change CN8 (usb) 12 pin board to board		11	1A	3B		
		Page26:Change CN5 footprint to cwy027-b0g1z-2p-1,CN16(USB)footprint change to usb-c107h6-10405-1-4p-r-v-nb4		12	1A			
		Page30:Change CN7 footprint to 4IN1-R015-212-LM-42P-H-nb4		13	1A			
		Page32:PJ1 footprint change to bat-btj-08qn0b-8p-r-v-nb4		14	3A			
		Page32:Del R510,change Hole15 footprint from h-tc315bc433d106p2 to h-tc315bsd106p2		15	2A			
		Page04:change C493 to no stuff		16	1A			
		Page27:Del T77 and Add R62		17	3A	3B		
		Page26:change Hole21 footprint to h-c236d142pt-8		18	2A			
		Page24:Change D1、D2、D3 footprint to led-ht-110nb5-3p		19	3A			
		Page24:Change R218,R234 to shortpad		20	1A			
		Page26:Change R310 to shortpad		21	3A			
		Page10:Change R91,R307,R418,R466,R469 to shortpad		22	1A			
		Page29:Add C466,C467 for EMI,Add R358,R357,R366,R367 and change DGND to LAN GND		23	3A			
		Page26:Add C716 for EMI		24	3A			
		Page30:Change L34 to 0 ohm and C715 to 10P,Change R512,R525,R528,R527 to 20K 1% and Change R526,R515,R524,R522 to 47K 1%		25	2A			
		Page25:Change R1,R4,R10,R365,R369,R368 to 221 ohm and Change D1,D2,D3 part number		26	3A			
		Page14:Change R282 to no stuff		27	2A			
		Page28:Change R26 to no stuff		28	3A			
		Page26:Change Hole29 part number to MBZR6005010		29	3A	3B		
		Page29:Del net name LAN_LNK_LED_PWR		30	1A			
		D	Page14:Add R583 and R315 at GPIO7 for HDMI option,change R583 to no stuff and R315 to stuff		31	3A		
			Page24:change HDMI item to no stuff(remove this function)		32	2A		
			Page12:change R225,R216,R241,R220,R219,R215,R213,R214,R228,R227 to no stuff for remove HDMI Audio		33	2A		
			Page26:Change Hole 16 footprint as hole1		34	2A		
					35	2A	3B	
					36	2A		
					37	2A		
		E	Page37:change PR97,PR98 to short-pad ,change PU4 OZ8116 change to OZ8111 for cost issue ,Del PC62		38	2A		
			Page27:C670 change value from 1U to 4.7U (CH5471M9907)		39	3A	3B	
			Page29:change c478 from 1000p to 220p.(CH122GK1I10)		40			
Page28:change C18 from 0.1u to 1000p (CH21006JB10),change C20 from 0.1u to 1u (CH5102K9B06) ,ADD C723 0.1u (CH41002KB93),ADD C720 1u (CH5102K9B06)								
Page25:change DHP00DA1G03->DHPTME53201								
Page24:add C722 (CH6101M9905) to solve ISN issue								
Page27:the PC beep will change Gain from -6db to -18 db , so R559 needs stuff 10k on all BOM.								
Page34:change PC133 from CC7560JMZ15 to CC7560JMZ02 for cost down								
Page36:change PC139 from CC7560JMZ15 to CC7560JMZ02 for cost down								
Page38:change PC156 from CC7560JMZ15 to CC7560JMZ02 for cost down								
Page33:change PC158,PC162 from CC73301MZB2 to CC73301MZ04 for cost down								
Page37:change PQ6,PQ7 from BAM700200F6 to BAM601K0003 for cost down								
MB Assy' P/N: 31ZR6MB0000/10/20/30/40/50/60/70			Project : ZR6 MB		Document No. :			
Approved by : Johnny_0		Drawing by :Andy Chen		DATE: 2009/03/04				

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Thermal Protection

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